Universidad Don Bosco.

Escuela de Estudios Tecnológicos.

"Sistema de Monitoreo Unidireccional por Telemetría. Parte de Transmisión."

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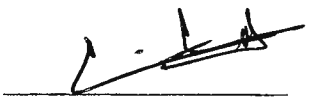

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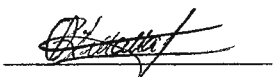

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Introducción.

En el siguiente trabajo de graduación se presenta un sistema de monitoreo unidireccional a larga distancia; se dice que es unidireccional porque el monitoreo de los parámetros será en una sola dirección y aunque se tendrá una visión general del comportamiento del equipo no podrá variarse el estado de éstos parámetros con el envío de una señal como respuesta, ya que simplemente se tendrá información del comportamiento general del equipo a monitorear; esto se realiza utilizando señales de radio a través del sistema de Telemetría, siendo éste aplicado al sistema de comunicación trunking.

Actualmente nuestro país ha entrado en un proceso de desarrollo tecnológico, en donde las telecomunicaciones está utilizando nuevas técnicas para obtener mayor rapidez en la comunicación así como una optimización del uso del espectro radioeléctrico, siendo el sistema ***trunking*** *el que ha dado mejores resultados.*

Este sistema ***trunking*** *consiste en un grupo de repetidoras, las cuales son controladas y administradas por un controlador central el cual asigna repetidoras sólo a las flotillas de unidades que requieren el uso de ellas. Estas repetidoras están ubicadas en un lugar de gran elevación con antena de gran ganancia con fines de aumentar la cobertura de la red de comunicación; en este modo toda transmisión efectuada por un radio es recibida por la repetidora y retransmitida por ésta misma a grandes distancias dadas sus características de mejor transmisión y recepción por lo que en este modo la cobertura es amplia con respecto a la cobertura limitada de los sistemas que no poseen una repetidora.*

En este modo de radiocomunicación si dos unidades están próximas, no por esto la comunicación será más clara ya que toda comunicación es canalizada a través de la repetidora.

Este trabajo de graduación está compuesto por : un sistema de transductores contenidos internamente en la planta que proporcionan un nivel de +12Vdc (marca) cuando se ha sobrepasado un nivel mínimo requerido para

que ésta funcione adecuadamente, los que serán tomados para modular una señal portadora por cada parámetro a monitorear; y luego transmitirlos por la radio-base desde el volcán de San Salvador (Picacho) hasta el departamento de Telecomunicaciones de la Policía Nacional Civil delegación Terminal de Oriente.

Este proyecto se ha dividido en dos etapas : Transmisión y Recepción. En este trabajo de graduación se presenta solamente la etapa de Transmisión. (Recepción está destinado para otro grupo que trabaja en forma paralela al nuestro, así al final, hacer la presentación de las dos etapas conjuntamente), y aunque tomando en cuenta que será necesario realizar ciertas pruebas de Transmisión, se planteará un esquema de lo que podría ser la etapa de Recepción, con el objetivo de no depender completamente del otro grupo y previendo con anticipación los contratiempos que tengan el grupo de Recepción.(Ver sección de Diagramas Electrónicos Esquemáticos).

Resumen del Proyecto a Realizar.

En la actualidad el uso de las Telecomunicaciones se ha hecho tan indispensable tanto así que la mayor parte de las empresas en nuestro país se han ligado a estos sistemas, porque son de gran importancia para su desarrollo.

La telemetría es utilizada como un medio de comunicación a larga distancia y es muy aplicada en la industria y el comercio obteniendo así mayor necesidad de implementar nuevos sistemas que ofrezcan mucha agilidad en el desarrollo de su ámbito de trabajo.

La función de este proyecto es sensar y convertir a señales radioeléctricas diferentes parámetros importantes de la planta tales como :

- ***Encendido o apagado de la máquina*** *(Shutdown) : es una salida que proporciona un voltaje constante de +12V (marca) cuando la planta ha sensado la presencia de la red comercial y así hacer la transferencia a ésta.*

- ***Alta temperatura de la planta*** *(High Engine Temperatura) : también es una salida que proporciona un nivel de +12 Vdc (marca) cuando el sensor ha detectado que la planta se ha sobrecalentado.*

- ***Baja presión del aceite*** *(Low Oil Presure) : salida que proporciona un voltaje constante de +12V (marca) cuando el nivel del aceite ha bajado demasiado de su nivel normal.*

- ***Bajo nivel de combustible*** *(Low Fuel-Output) : salida que proporciona un nivel de +12Vdc cuando el sensor del nivel de combustible ha detectado que el combustible ha bajado hasta el nivel mínimo permitido.*

La planta a monitorear es de la marca ***Cummins.Onan.Genset Model.*** *Esta posee un panel de control donde se encuentran disponibles todas las salidas antes mencionadas.(Ver ANEXO A.11)*

Luego habiendo sensado los parámetros éstos serán convertidos de voltaje a frecuencia utilizando un tipo de modulación digital con portadora

analógica que se conoce como ***Conmutación de Corrimiento de Amplitud (ASK : amplitud-shift keyin)*** *el que consiste en que la amplitud de la señal portadora de alta frecuencia se alterna entre dos o más valores en respuesta al código PCM. En el caso binario, la elección habitual es el conmutador encendido-apagado (abreviado a veces OOK). La onda de amplitud modulada resultante consiste en pulsos RF, llamados* ***marcas****, que representan al binario 1, y* ***espacios*** *que representan al binario 0. En la figura 1 se muestra una onda ASK para un código PCM dado. Como en la AM, el ancho de banda se duplica en el ASK. La onda ASK para un pulso (es decir, un binario) puede escribirse :*
$\phi(t) = A \operatorname{sen} wt$, *para* $0 < t < T$; *y* 0, *para cualquier otro caso.*

Figura 1
Onda Binaria ASK.

Así la señal portadora será generada por medio de un VCO en modo de oscilación libre es decir funcionará como un simple generador de funciones sintonizado a una única frecuencia la que será modulada por la señal mensaje proveniente del puerto de salida del panel de control interno de la planta; que proporciona un nivel (marca), cuando el sensor ha detectado que el parámetro a monitorear ha sobrepasado el nivel mínimo requerido ,todo esto se repetirá por cada uno de los parámetros a monitorear. Luego esta información será transmitida por medio de los transceptores Radios-Base ***Max Trac 888****, los cuales facilitan mucha rápidez y mínimos porcentajes de error en pérdidas de señal causadas por medios externos.*

El radio que se utilizará para la transmisión de los parámetros no estará continuamente como transmisor sino que alternará la función de transmisor y receptor con el objetivo de que no se sobrecaliente ya que cuando realiza la función de transmisor es cuando absorbe la mayor potencia de la batería, este cambio se realiza por medio del botón de transmisión ubicado en el micrófono llamado PTT, al presionar este botón el voltaje de CD se transfiere de la etapa de recepción a la de transmisión, eliminando la operación simultánea de receptor y transmisor. El radio puede estar permanente como receptor y no calentarse por lo que el radio donde se recibirán los parámetros a monitorear siempre permanecerá como receptor.

Objetivo General.

- *Implementar un prototipo de un sistema de monitoreo unidireccional utilizando la Telemetría.*

Objetivos Específicos.

- *Optimizar el equipo de Radiocomunicaciones en el Departamento de Telecomunicaciones de la Policía Nacional Civil para solventar una necesidad específica y así plasmar los conocimientos adquiridos a nivel Tecnológico.*

- *Tener una visión panorámica del comportamiento del equipo a monitorear.*

- *Aumentar el control del funcionamiento y estado de operación del equipo favoreciendo la aplicación de un buen mantenimiento preventivo y correctivo.*

Explicación del Proyecto por Bloques.

NOTA: Referirse a los diagramas electrónicos esquemáticos contenidos al final de esta sección, páginas xvi, xvii y xviii, donde se encuentran divididos los bloques por líneas punteadas.

- ***Generadores de Portadoras:*** *consiste en generar por medio de un VCO una señal sinusoidal pura (tono) una por cada parámetro a monitorear y a diferentes frecuencias diferentes entre sí; que servirán como señal portadora. Esto se hace con un circuito integrado que funcionará como generador de funciones (ICL 8038). El diagrama esquemático del ICL8038, así como muchos datos de fabricación se presentan en las hojas técnicas del ANEXO A.1.*

  Un VCO es un circuito que proporciona una señal de salida oscilante (senoidal, cuadrada o triángular) cuya frecuencia puede ajustarse dentro de un rango determinado por un voltaje de DC.

  Es posible obtener una señal simétrica (con Duty Cycle=50%) si se escoge el valor de los resistores RA=RB=R, (Ver figura A.1); aunque hay otras formas de conectar estos resistores. Con los dos resistores separados la frecuencia está dada por. ***f=0.33/R.C***

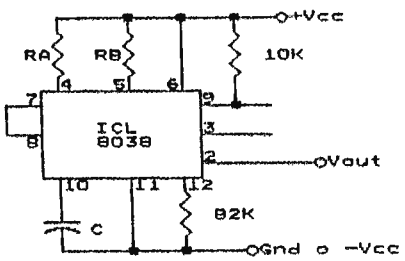


Figura A.1
ICL 8038.
Generador de funciones.

Para la generación de las portadoras utilizadas en el proyecto se presentan los siguientes cálculos:

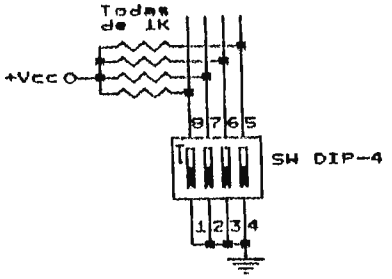
$f1 = 0.33/R.C = 0.33/(10K).(0.033uF) = 1\ KHz$

$f2 = 0.33/R.C = 0.33/(6.5K).(0.033uF) = 1.5\ KHz$

$f3 = 0.33/R.C = 0.33/(5K).(0.033uF) = 2\ KHz$

$f4 = 0.33/R.C = 0.33/(4K).(0.033uF) = 2.5\ KHz$

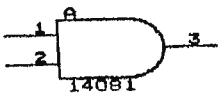
- ***Simuladores de Señal Mensaje:*** *comprende los niveles de salida de los parámetros a monitorear de la planta como son: temperatura de la máquina, baja presión del aceite, bajo nivel del combustible, y el apagado-encendido de la máquina, niveles que servirán para modular a la portadora analógica generada por cada parámetro dejándola pasar o no al radio-base. Para efectos de la presentación de la defensa la señal mensaje se simulará con la ayuda de los microswicht.*



- ***Habilitadores:*** *comprende una compuerta AND de dos entradas por cada parámetro a monitorear, que trabajará conjuntamente con el decodificador, y con la señal mensaje proveniente de los microswicht, así pues si la compuerta AND contiene unos lógicos en sus dos entradas cerrará los contactos de los swicth analógicos dejando pasar el tono directamente hacia el transmisor. (Ver figura A.2)*

El MC14081B se trata de un CI de Lógica CMOS , en un encapsulado de 14 pines. Este contiene 4 compuertas AND de dos entradas cada una.

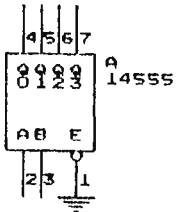
Figura A.2
Compuerta AND.



- ***Decodificador:*** *servirá para habilitar una de las compuertas AND a la vez, colocándole un uno lógico según sea la cuenta de los dos bits menos significativos del contador binario.(Ver figura A.3).*

EL MC14555B se trata de un CI de Lógica CMOS , en un encapsulado de 16 pines. Este contiene dos decodificadores de dos a cuatro líneas con salida en alto.

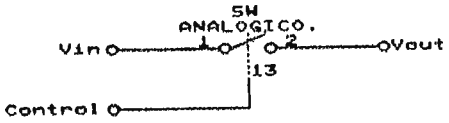
Figura A.3
Decodificador.



- ***Switch Analógicos:*** *serán activados por la salida de las compuertas AND, y tendrán como objetivo el de poner o no la señal de portadora (tono) a la salida. (Ver figura A.4).*

El MC14066B es un CI de lógica CMOS, en un encapsulado de 14 pines. Este contiene 4 switch analógicos con un pin destinado al cierre de cada switch (activo alto).

Figura A.4
Switch Analógico.



- ***Habilitador del PTT:*** *consiste en una compuerta OR de 4 entradas que dará el estado de alarma con una de las condiciones de la señal mensaje que se cumpla, este estado presente es el que se enganchará y servirá para llevar a corte o saturación al transistor ocupado como interruptor que cerrará los contactos del relé para la posterior activación del PTT.*

El MC14072B se trata de un CI de lógica CMOS , en un encapsulado de 14 pines. Este contiene 2 compuertas OR de cuatro entradas cada una.(Ver figura A.5)

Figura A.5
Habilitador del PTT.

- ***Reloj:*** *es un integrado que actuará en modo de operación astable y que proporcionará la señal de temporización para la cuenta ascendente incrementándolo con su transición positiva; con un período de duración entre cuenta y cuenta de alrededor de 2 segundos.(Ver figura A.6).*

El LM 555 es un temporizador que puede considerarse como un conjunto funcional que tiene dos comparadores, dos transistores, tres resistencias iguales, un flip-flop y la etapa de salida. El temporizador CI 555 tiene dos modos de operación, ya sea como un multivibrador Astable (de oscilación libre) ó como un multivibrador Monostable (un disparo). Para el caso, la operación en oscilación libre del CI 555 es de mayor relevancia en la realización del presente proyecto.

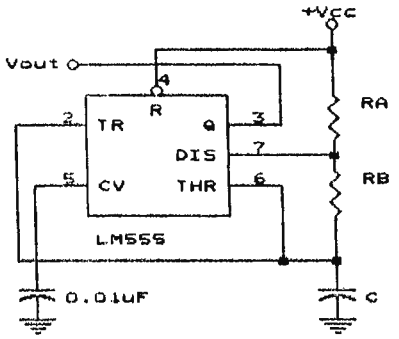


Figura A.6
LM 555 en modo Astable.

La salida permanece alta durante el intervalo de tiempo en que C se carga desde 1/3.Vcc a 2/3.Vcc. Este intervalo está dado por :

$$\boldsymbol{Talto = (RA+RB)\ .\ C\ .\ ln\ 2}$$

La salida está baja durante el intervalo en que C se descarga de 2/3.Vcc a 1/3.Vcc y está dado por :

$$\boldsymbol{Tbajo = RB\ .\ C\ .\ ln\ 2}$$

Así el período total de oscilación T es :

$$\boldsymbol{T = Talto+Tbajo = (RA+2RB)\ .\ C\ .\ ln\ 2}$$

La duración del período ocupado en el proyecto es:

1. *Para la parte de TX:*
   $T = (RA+2RB).C.ln\ 2 = [(1K)+(2).(1K)].1000uF.ln\ 2 = 2\ Seg.$
2. *Para la parte de RX:*
   $T = (RA+2RB).C.ln\ 2 = [(1K)+(2).(1K)].470uF.ln\ 2 = 1\ Seg.$

- ***Contador Binario Ascendente:*** *su cuenta en los 2 bits menos significativos dará la activación de una compuerta AND a la vez con la ayuda del decodificador; así como también dará la cuenta para los decodificadores de inicio de cuenta y de media cuenta para hacer el cambio de TX a RX por medio del PTT. (Ver figura A.7).*

El MC14520B se trata de un contador síncrono de Lógica CMOS , en un encapsulado de 16 pines. Este contiene dos contadores binarios (de 4 bits) ascendentes.

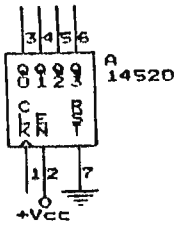


Figura A.7
Contador Binario Ascendente.

- ***Decodificador para inicio/media cuenta:*** *sus estados servirán para la activación del PTT del Radio-Base, el decodificador de media cuenta hará que el radio se mantenga como transmisor durante la cuenta de 8h a Fh, luego entrará el decodificador de inicio de cuenta que hará pasar al radio-base a la función de receptor durante la cuenta de 0h a 7h.*

- ***Atenuador:*** *contiene un Amp-Op en configuración de amplificador inversor tanto en la parte de TX como de RX con una ganancia inferior a uno para que el nivel de entrada en el radio-base sea de alrededor de 150mV RMS. (Ver figura A.8)*

En el caso particular del presente proyecto, se utilizan amplificadores operacionales para tener completo dominio de la ganancia de las señales analógicas a transmitir.

La configuración del Amplificador Operacional utilizada en el proyecto es como : ***Amplificador Inversor****. Es un amplificador cuya ganancia en lazo cerrado desde Vi a Vo está dada por Rf y Ri. Puede amplificar señales de CA o CD. Para entender como opera, se hacen dos superposiciones de simplificación apegadas a la realidad.*

✓ *La diferencia de voltaje entre las terminales de entrada (+) y (-) es esencialmente 0, si Vo no está en saturación.*

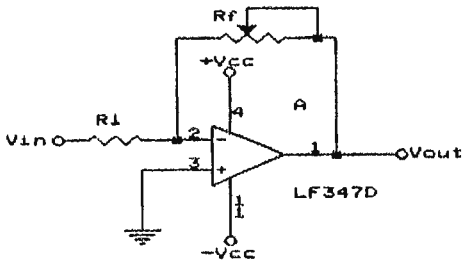
✓ *La corriente requerida por las terminales de entrada (+) y (-) es despreciable.*

Tomando en cuenta los puntos anteriores, se plantean igualdades matemáticas que conducen a la ecuación del Amplificador Inversor:

$$Vo = (-Rf/Ri).Vi$$

El LF 347 es un CI de encapsulado de 16 pines que contiene 4 amplificadores operacionales con entrada JFET de bajo ruido y compensación interna de frecuencia así como bajo nivel de offset.

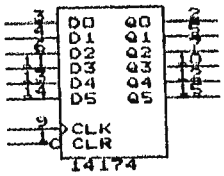
Figura A.8
Atenuador.



- ***Enganchador de Estado:*** *consiste en unos FF tipo D (latch) que servirán para enganchar con ayuda del decodificador de media cuenta e inicio de cuenta el estado de alarma presente a la salida del habilitador del PTT (OR de 4 entradas) que en sí proporcionará el corte o la saturación del transistor utilizado como interruptor que en consecuencia cerrará los contactos del PTT.*

La operación del Latch es muy simple; Q pasará al mismo estado que está presente en la entrada D cuando ocurre una transición positiva en CLK.

Figura A.9
Enganchador de Estado.



Nótese que cada vez que una transición positiva ocurre en la entrada CLK, Q toma el valor presente en la entrada D. Las transiciones en sentido negativo en CLK no tienen efecto y la entrada D no tiene efecto excepto cuando ocurre una transición positiva.

Los multivibradores biestables D con transición negativa activada se encuentran disponibles también y operan exactamente en la misma forma, a excepción que responden sólo a transiciones negativas en la entrada CLK. El símbolo para estos FF tendrá un pequeño círculo en la entrada CLK.

El MC140174B se trata de un CI de lógica CMOS , en un encapsulado de 16 pines. Este contiene 6 FF tipo D activados con transición positiva, no posee salida complementaria pero si posee un pin de reset activo en bajo. (Ver figura A.9).

- ***Interruptor-Relé:*** *contiene un transistor NPN ocupado como interruptor que según su entrada cerrará los contactos del relé para activar al radio-base como transmisor por medio de los contactos del PTT.(Ver figura A.10)*

El ocupar un transistor como un interruptor, significa que debe operarse en el punto de saturación o de corte y no en alguna otra parte de la trayectoria de la linea de carga de DC. Cuando un transistor se satura, actúa como un interruptor cerrado entre el colector y el emisor. Cuando un transistor está en corte, actúa como interruptor abierto.

La corriente de base I_B está dada por.

$$I_B = (V_{BB} - V_{BE})/R_B.$$

$$I_B = (12V - 0.7V) / 10K = 1.13\ mA.$$

$$I_{csat} = \beta . I_B = 200.(1.13mA) = 226mA.$$

Si la corriente de base es mayor o igual a $I_{B(sat)}$, el punto de operación Q está en la parte superior de la linea de carga. En este caso, el transistor actúa como interruptor cerrado. Por otra parte, si la corriente de base es cero, el transistor opera en la parte inferior de la linea de carga y actúa como un interruptor abierto.

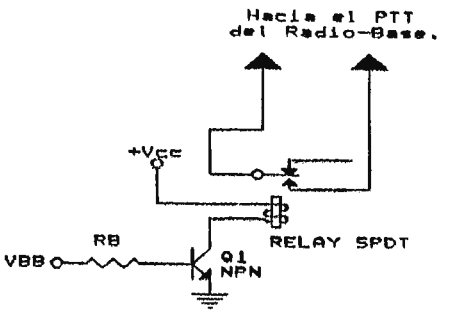


Figura A.10
Interruptor-Relé.

- ***Detectores de Portadora:*** *consiste en cuatro PLL's (Lazo de fase Cerrada) CI LM 567 llamados generalmente decodificador de tono; diseñados específicamente para detectar una frecuencia determinada. Consta de un Oscilador Controlado por Voltaje, un detector de fase, y un detector auxiliar en cuadratura. La frecuencia central del decodificador de tono y ancho de banda se especifican mediante su frecuencia de oscilación libre y el rango de captura.(Ver figura A.11)*

fo = 1/ (1.1 R1.C1) *: frecuencia central.*
BW = 1070 . [Vi / (fo.C2)]^1/2 *: ancho de banda (en % de fo)*

donde: *Vi : Voltaje de entrada (< 200mVrms)*
C2 : Capacitancia en el pin 2 (uF).

Para el presente proyecto los cálculos son:
fo1 = 1/ [(1.1).(9.1K).(0.1uF)] = 1 KHz.
fo2 = 1/ [(1.1).(6K).(0.1uF)] = 1.5 KHz.
fo3 = 1/ [(1.1).(4.5K).(0.1uF)] = 2 KHz.
fo4 = 1/ [(1.1).(3.6K).(0.1uF)] = 2.5 Khz.

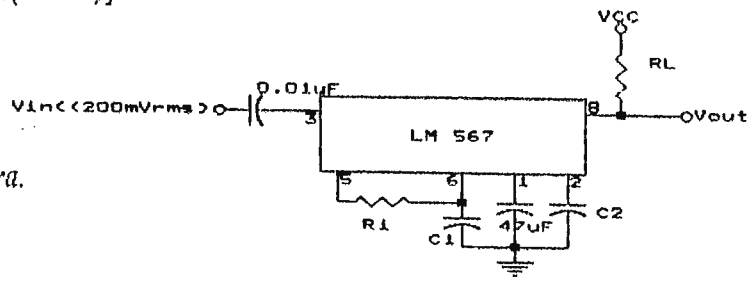


Figura A.11
Detector de Portadora.

- ***Presentadores:*** *se encargarán de presentar el estado de salida de los PLL's en unos LED's indicando la posible detección de la portadora; con la ayuda de los Latch que engancharán dichos estados. (Ver figura A.12)*

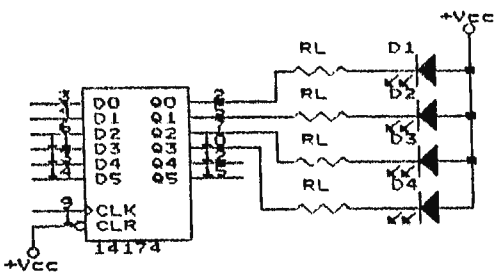


Figura A.12
Presentadores.

- ***Radio-Base Transmisor y Receptor :*** *El radio Max Trac 888 opera en la banda de 806-821 y 851-870 MHz para la transmisión y en la banda de 851-870 MHz para la recepción (Ver figura A.13). A continuación se enumeran algunas de las cacterísticas del radio más importantes: 20 canales de operación, 2 display de caracteres, botón de transmisión PTT, 15 watt de potencia de salida, alimentación de +12Vd, reloj de tiempo fuera (Timer),etc.*

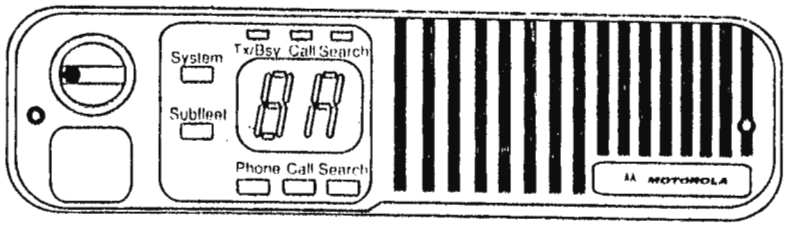


Figura A.13
Radio-Base Max Trac 888.

Un Sistema de Radio Troncalizado permite un gran número de usuarios que se distribuyen relativamente en un pequeño número de frecuencias. Cuando el usuario aprieta el botón (PTT) para establecer una comunicación con otro usuario siempre en el mismo sistema, el sistema automáticamente asigna un camino y una repetidora en esta frecuencia. Tan pronto como la conversación finaliza la repetidora es liberada para otros usuarios. Los sistemas troncalizados de radios Motorola tienen un controlador central, la cual asigna frecuencias automáticamente y una repetidora por cada frecuencia usada. Al llevar un control de las frecuencias asignadas a las repetidoras se logra evitar congestionamientos en los canales. Solamente requiere un intento para accesar al sistema. Si todos los canales estan ocupados, el requisito de llamado entra a una fila y la controladora central asigna automáticamente el próximo canal disponible y un tono de "dih-dih-dih" suena cuando la llamada puede ser hecha.

Resumen de Caracteres en el Display: *El Max Trac 888 tiene 2 displays numéricos, con capacidad de representar algunas letras, pero no se considera un verdadero display alfanumérico.*

Visualizador Operacional.

[#_]	*Un número en el display izquierdo indica el sistema/flota y puede ser de 1 a 6.*
[_A]	*Una letra en la posición derecha indica la subflota y puede ser A,B,C.*
[##]	*Un número si una letra indica un canal convencional y puede ser del 1 al 6.*

Encendido del Radio: *Se enciende en la perilla de volumen girándolo en el sentido de las agujas del reloj. El display se iluminará y en el radio sonará un simple beep.*

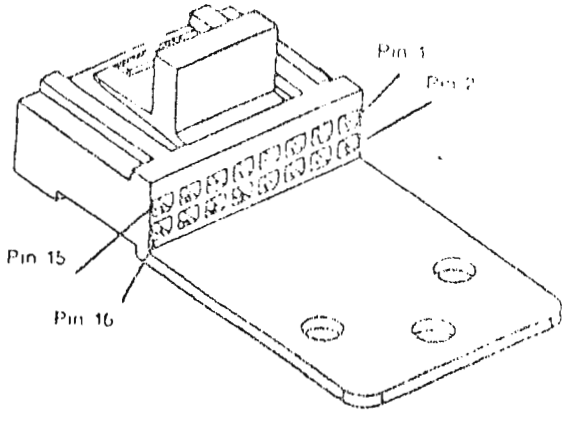
Para Recibir: *Seleccione el sistema presionando el botón [system] hasta que el número del sistema sea desplegado. Para seleccionar subflota presione el botón [subflect] hasta que la letra de la subflota sea mostrada. Un sistema convencional presentará un número sin tener un caracter o letra. Un sistema troncalizado siempre tendrá una letra o un caracter especial al lado derecho del display.*

Para Transmitir durante la operación de un sistema Troncalizado: *Cuando la luz del led indicador del transmisor encienda, presione PTT y hable por el microfono con una voz normal. Si escucha tono(s) cuando presione el PTT; el sistema está alertándolo sobre ciertas condiciones existentes. Referirse a los tonos de alerta para su explicación.*

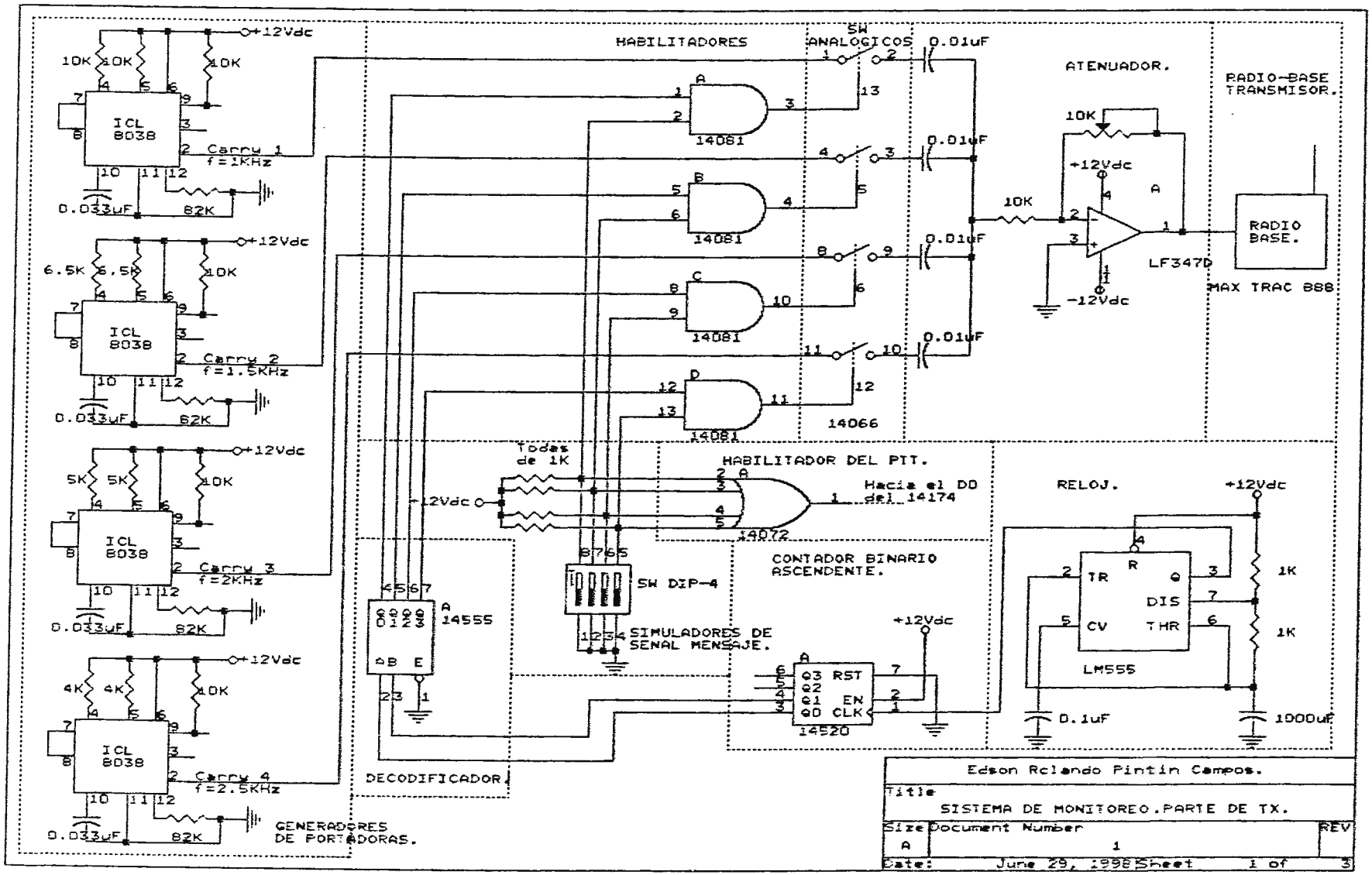
Para Transmitir durante la operación sobre un Sistema Convencional: *No transmitirá si alguien está usando el canal. Cuando presione el PTT contenido en el microfono el indicador de transmisión será encendido continuamente para indicarle que esta "en el aire". Quedara encendido hasta que el botón de el PTT sea liberado.*

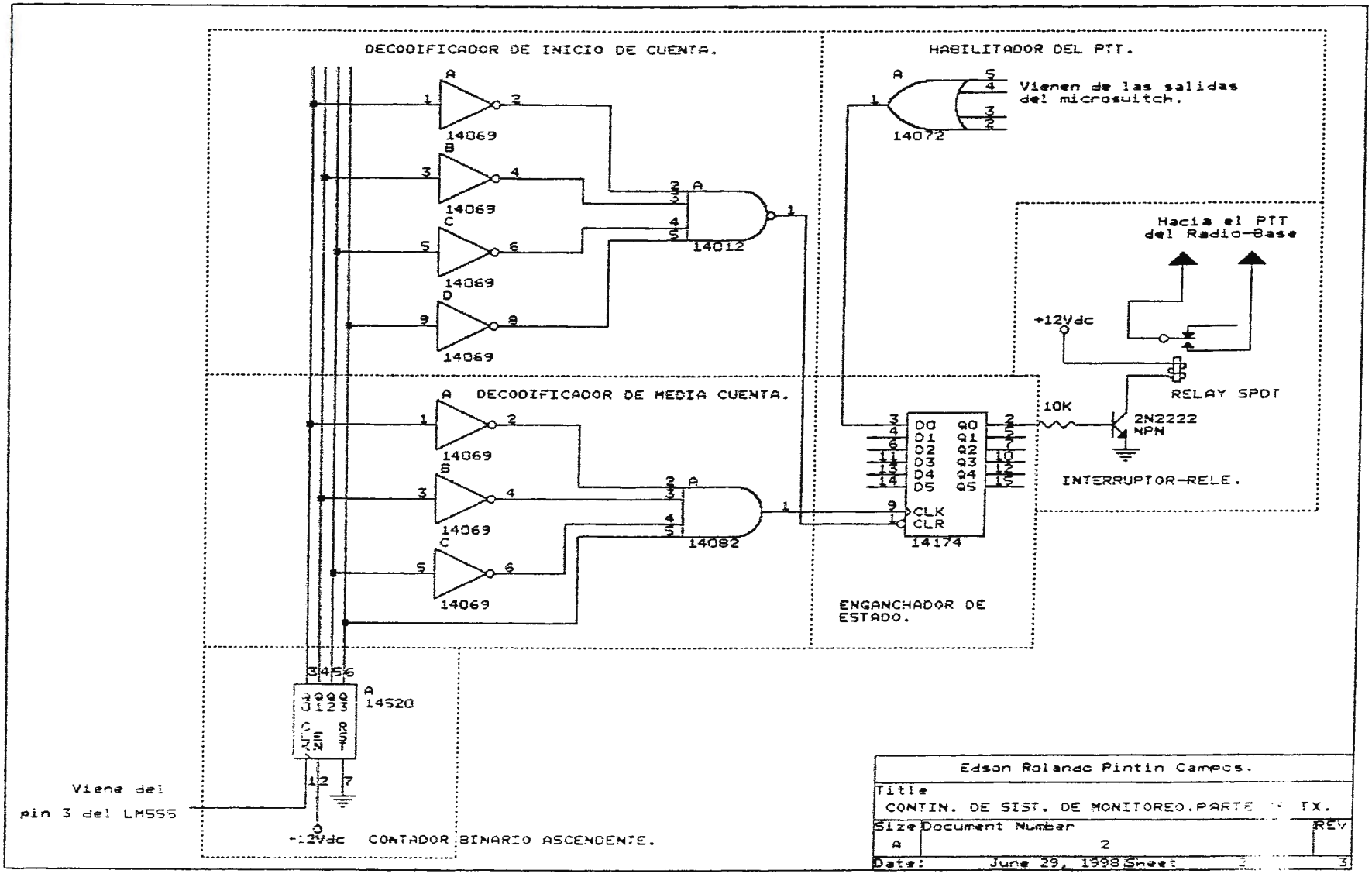
Conector para la Expansión de Accesorios: *Esta parte provee salidas y entradas de las diferentes funciones que realizan las Radio-Bases que será adonde se introducirá la información (pin 5 y 7) al igual que se hará el cambio de transmisor a receptor por medio del pin de PTT (pin 3 y 7) en el radio transmisor; y también se obtendrán la información de salida en el radio receptor (pin 11 y 7) contenidos todos sobre el conector para la expansión de accesorios.(Ver siguiente cuadro y figura)*

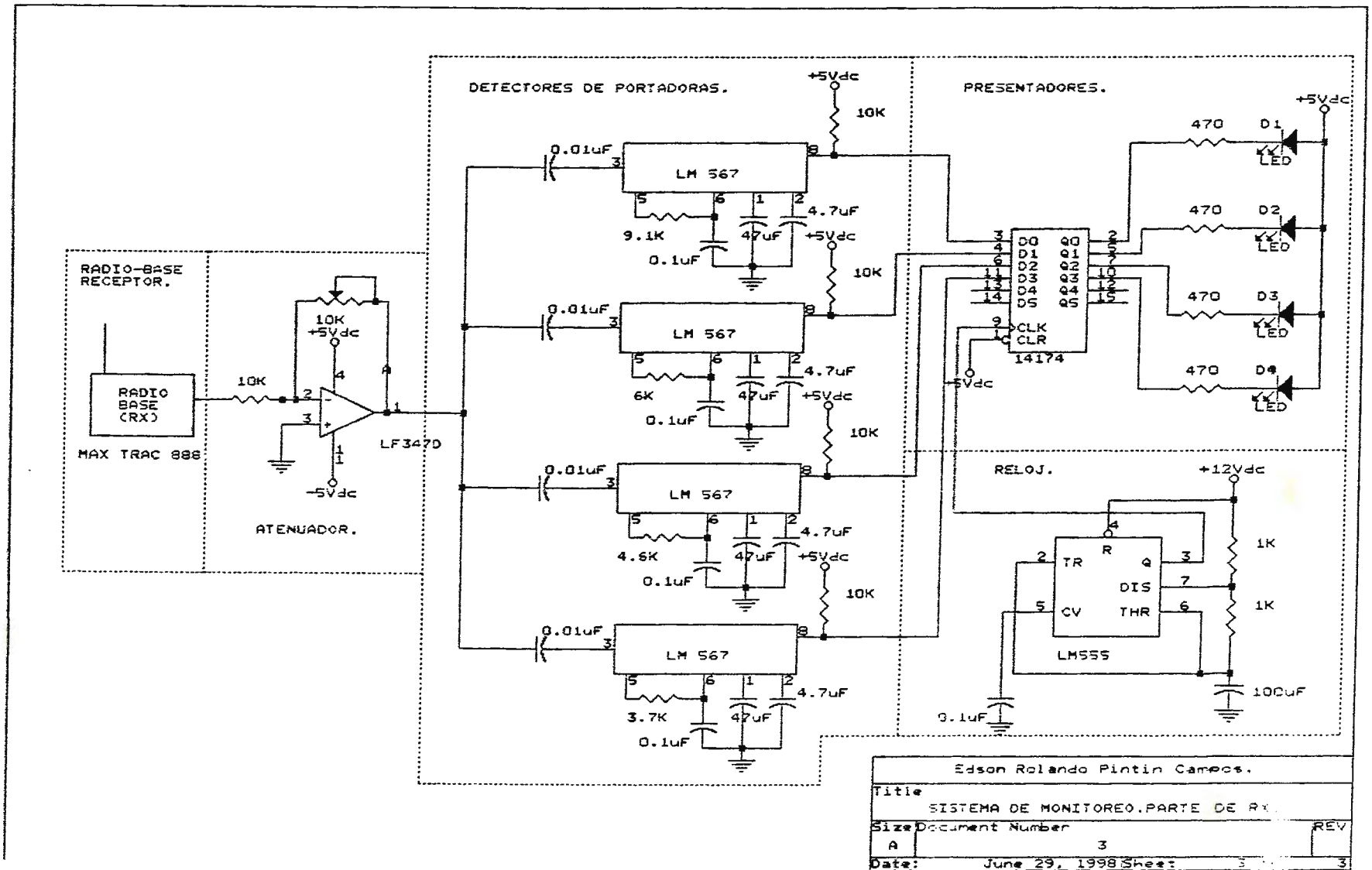
Pin Number	Description
1	External Speaker Negative.
2	Microphone Audio 80mVrms @ 3KHz Desviation
3	Microphone PTT
4	Programmable-See Radio Service Software.
5	Flat Transmit Audio 150mVrms @ 3KHz Desviation
6	Programmable-See Radio Service Software.
7	Ground
8	Programmable-See Radio Service Software.
9	Emergency Alert Input.
10	Ignition Control Input.
11	Discriminator Audio Output 350mVrms @ 3khz Desviation
12	Programmable-See Radio Service Software.
13	Switched A+ Sense 0.5 Amps. Max.
14	Programmable-See Radio Service Software.
15	Internal Speaker Positive
16	Internal Speaker Negative.



Diagramas Electrónicos Esquemáticos.


+12Vdc
10K
ICL 8038
Carry 1 f=1KHz
0.033uF
82K
6.5K
Carry 2 f=1.5KHz
5K
Carry 3 f=2KHz
4K
Carry 4 f=2.5KHz
GENERADORES DE PORTADORAS.
HABILITADORES
SW ANALOGICOS
0.01uF
14081
14066
ATENUADOR.
LF347D
-12Vdc
RADIO-BASE TRANSMISOR.
RADIO BASE.
MAX TRAC 888
Todas de 1K
HABILITADOR DEL PIT.
Hacia el DD del 14174
14072
SW DIP-4
SIMULADORES DE SEÑAL MENSAJE.
14555
DECODIFICADOR
CONTADOR BINARIO ASCENDENTE.
Q3 RST
Q2
Q1 EN
Q0 CLK
14520
RELOJ.
TR
R
Q
DIS
CV
THR
LM555
1K
0.1uF
1000uF
Edson Rolando Pintin Campos.
Title
SISTEMA DE MONITOREO.PARTE DE TX.
Size A
Document Number 1
REV
Date: June 29, 1998 Sheet 1 of 3


DECODIFICADOR DE INICIO DE CUENTA.
HABILITADOR DEL PTT.
Vienen de las salidas del microsuitch.
14072
14069
14012
Hacia el PTT del Radio-Base
+12Vdc
RELAY SPDT
10K
2N2222 NPN
INTERRUPTOR-RELE.
DECODIFICADOR DE MEDIA CUENTA.
14082
14174
CLK
CLR
ENGANCHADOR DE ESTADO.
14520
Viene del pin 3 del LM555
+12Vdc
CONTADOR BINARIO ASCENDENTE.
Edson Rolando Pintin Campos.
Title
CONTIN. DE SIST. DE MONITOREO.PARTE DE TX.
Size
A
Document Number
2
REV
Date: June 29, 1998 Sheet 3 of 3


DETECTORES DE PORTADORAS.
PRESENTADORES.
RADIO-BASE RECEPTOR.
RADIO BASE (RX)
MAX TRAC 888
10K
+5Vdc
-5Vdc
LF347D
ATENUADOR.
0.01uF
LM 567
9.1K
6K
4.6K
3.7K
0.1uF
4.7uF
47uF
470
D1
D2
D3
D4
LED
14174
D0
D1
D2
D3
D4
D5
Q0
Q1
Q2
Q3
Q4
Q5
CLK
CLR
RELOJ.
+12Vdc
LM555
TR
R
Q
DIS
CV
THR
1K
100uF
Edson Rolando Pintin Cameos.
SISTEMA DE MONITOREO.PARTE DE RX
Size
A
Document Number
3
REV
Date: June 29, 1998 Sheet 3 of 3

ANEXO A. Hojas Técnicas de Dispositivos Electrónicos.

ICL8038

Precision Waveform Generator/Voltage Controlled Oscillator

INTERSIL

GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

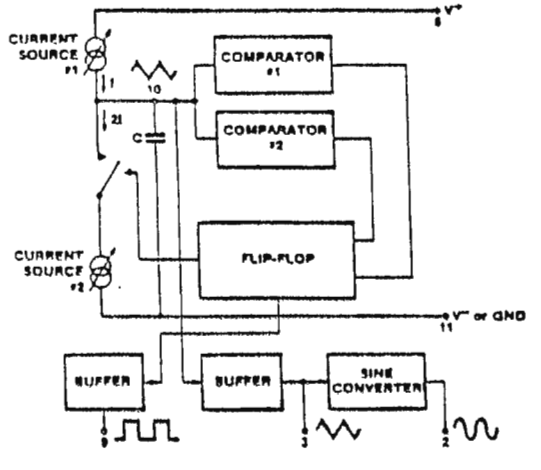
FEATURES

- Low Frequency Drift With Temperature — 250ppm/°C
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Low Distortion — 1% (Sine Wave Output)
- High Linearity — 0.1% (Triangle Wave Output)
- Wide Operating Frequency Range — 0.001Hz to 300kHz
- Variable Duty Cycle — 2% to 98%
- High Level Outputs — TTL to 28V
- Easy to Use — Just A Handful of External Components Required

ORDERING INFORMATION

Part Number	Stability	Temp. Range	Package
ICL8038CCPD	250ppm/°C typ	0°C to + 70°C	14 pin MiniDIP
ICL8038CCJD	250ppm/°C typ	0°C to + 70°C	CERDIP
ICL8038BCJD	180ppm/°C typ	0°C to + 70°C	CERDIP
ICL8038ACJD	120ppm/°C typ 110	0°C to + 70°C	CERDIP
ICL8038BMJD*	350ppm/°C max	−55°C to + 125°C	CERDIP
ICL8038AMJD*	250ppm/°C max	−55°C to + 125°C	CERDIP

*Add /883B to part number if 883 processing is required.



0328-1

Figure 1: Functional Diagram

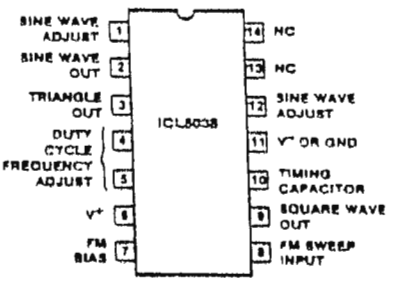


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Figure 2: Pin Configuration (Outline dwg JD)

302600-002

NOTE: All typical values have been characterized but are not tested.

ICL8038

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^- to V^+) 36V
Power Dissipation[1] 750mW
Input Voltage (any pin) ..... V^- to V^+
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range:
8038AM, 8038BM ..... −55°C to +125°C
8038AC, 8038BC, 8038CC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified)

Symbol	General Characteristics	8038CC			8038BC(BM)			8038AC(AM)			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{SUPPLY}	Supply Voltage Operating Range										
V^+	Single Supply	+10		+30	+10		30	+10		30	V
V^+, V^-	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I_{SUPPLY}	Supply Current (V_{SUPPLY} = ±10V)[2]										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
Frequency Characteristics (all waveforms)											
f_{max}	Maximum Frequency of Oscillation	100			100			100			kHz
f_{sweep}	Sweep Frequency of FM Input		10			10			10		kHz
	Sweep FM Range[3]		35:1			35:1			35:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
$\Delta f/\Delta T$	Frequency Drift With Temperature[5] 8038 AC, BC, CC 0°C to 70°C		250			180			120		ppm/°C
	8038 AM, BM, −55°C to 125°C						350			250	ppm/°C
$\Delta f/\Delta V$	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V
Output Characteristics											
I_{OLK}	Square-Wave Leakage Current (V_O = 30V)			1			1			1	µA
V_{SAT}	Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
t_r	Rise Time (R_L = 4.7kΩ)		180			180			180		ns
t_f	Fall Time (R_L = 4.7kΩ)		40			40			40		ns
ΔD	Typical Duty Cycle Adjust (Note 6)	2		98	2		98	2		98	%
$V_{TRIANGLE}$	Triangle/Sawtooth/Ramp Amplitude (R_{TRI} = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPPLY}
	Linearity		0.1			0.05			0.05		%
Z_{OUT}	Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
V_{SINE}	Sine-Wave Amplitude (R_{SINE} = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPPLY}
THO	THO (R_S = 1MΩ)[4]		2.0	5		1.5	3		1.0	1.5	%
THO	THO Adjusted (Use Figure 8)		1.5			1.0			0.8		%

NOTES: 2. R_A and R_B currents not included.
3. V_{SUPPLY} = 20V; R_A and R_B = 10kΩ, f = 10kHz nominal; can be extended 1000 to 1. See Figures 7a and 7b.
4. 82kΩ connected between pins 11 and 12. Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
5. Figure 3, pins 7 and 8 connected. V_{SUPPLY} = ±10V. See Typical Curves for T.C. vs V_{SUPPLY}.
6. Not tested, typical value for design purposes only.

NOTE: All typical values have been characterized but are not tested.

TEST CONDITIONS

Parameter		R_A	R_B	R_L	C_1	SW_1	Measure
Supply Current		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Sweep FM Range(1)		10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Frequency Drift with Supply Voltage(2)		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude: (Note 4)	Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
	Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off)(3)		10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on)(3)		10kΩ	10kΩ		3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times (Note 5)		10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust: (Note 5)	MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
	MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTES: 1. The HI and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{HI}) and then connecting pin 8 to pin 6 (f_{LO}). Otherwise apply Sweep Voltage at pin 8 ($\frac{2}{3}$ V_{SUPPLY} + 2V) ≤ V_{SWEEP} ≤ V_{SUPPLY} where V_{SUPPLY} is the total supply voltage. In Figure 7b, pin 8 should vary between 5.3V and 10V with respect to ground.

2. 10V ≤ V^+ ≤ 30V, or ±5V ≤ V_{SUPPLY} ≤ ±15V.

3. Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.

4. Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to −5.0V.

5. Not tested; for design purposes only.

DEFINITION OF TERMS:

Supply Voltage (V_{SUPPLY}). The total supply voltage from V^+ to V^-

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$(\tfrac{2}{3}\ V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$$

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

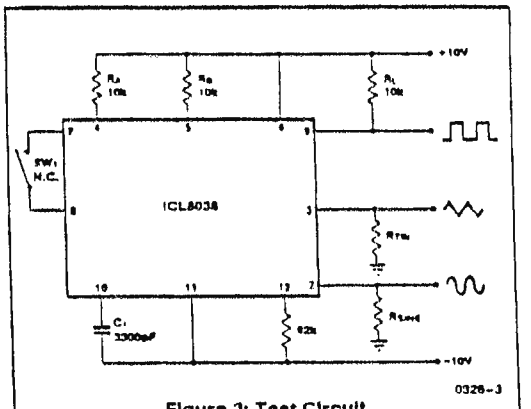


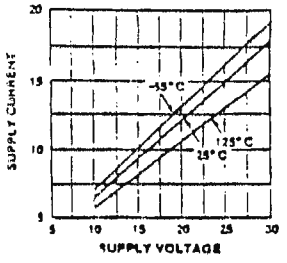
Figure 3: Test Circuit

NOTE: All typical values have been characterized but are not tested.

ICL8038

INTERSIL

TYPICAL PERFORMANCE CHARACTERISTICS



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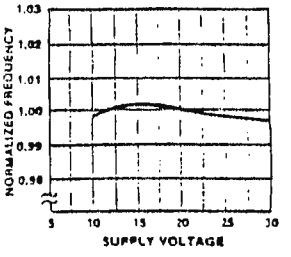
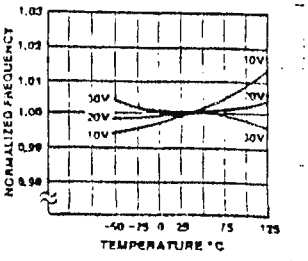
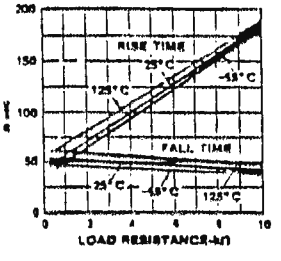


0328-5

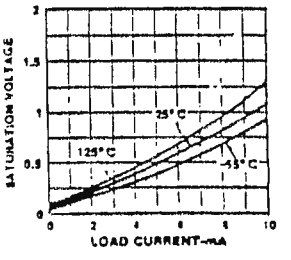


0328-6

Performance of the Square-Wave Output

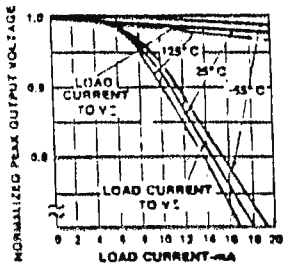


0328-7

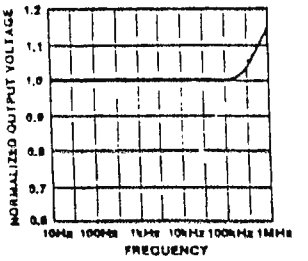


0328-8

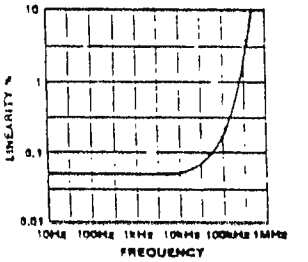
Performance of Triangle-Wave Output



0328-9

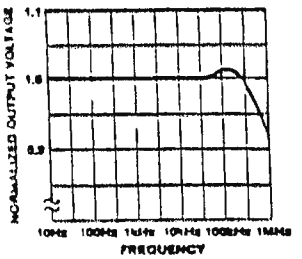


0328-10

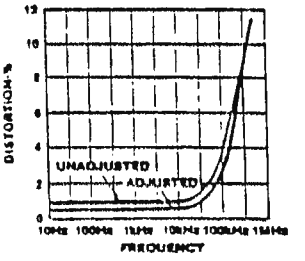


0328-11

Performance of Sine-Wave Output

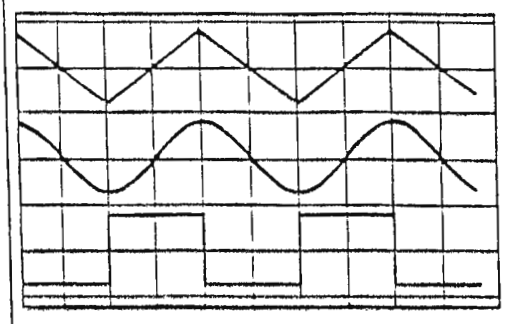


0328-12



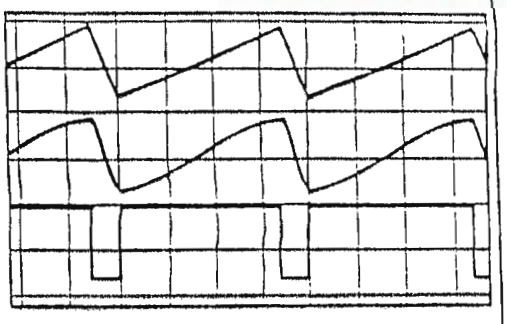
0328-13

NOTE: All typical values have been characterized but are not tested.



0326-14

Square-Wave Duty Cycle — 50%



0325-15

Square-Wave Duty Cycle — 80%

Figure 4: Phase Relationship of Waveforms

DETAILED DESCRIPTION (See Figure 1)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at ⅔ of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at ⅓ of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 5. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at ⅓ V_{SUPPLY}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} V_{SUPPLY}}{2(0.22)\frac{V_{SUPPLY}}{R_B} - 0.22\frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 5b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 5c. This connection, however, causes an inherently larger variation of the duty-cycle, frequency, etc.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66}\left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 5a)}$$

If a single timing resistor is used (Figure 5c only), the frequency is

$$f = \frac{0.165}{RC}$$

NOTE: All typical values have been characterized but are not tested.

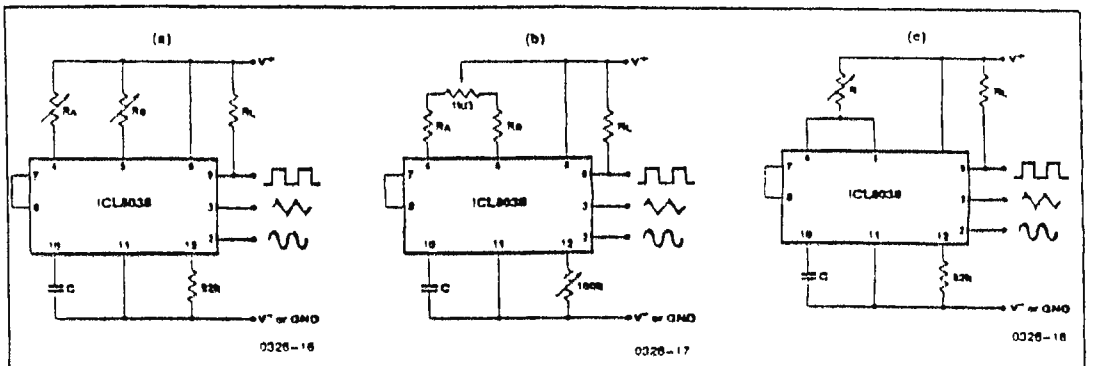


Figure 5: Possible Connections for the External Timing Resistors

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.

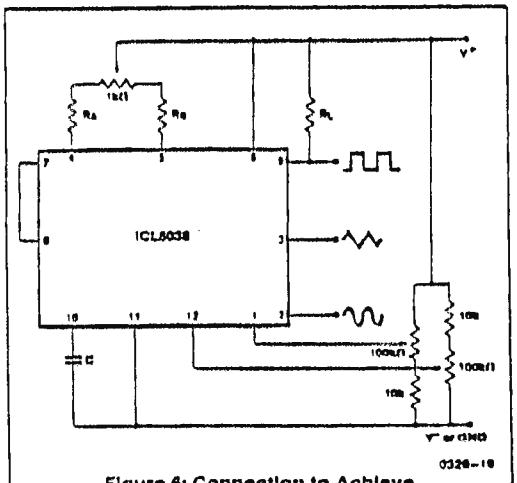


Figure 6: Connection to Achieve Minimum Sine-Wave Distortion

SELECTING R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times (V^+ - V^-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V^+ - V^-)}{R_A}$$

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V^+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

NOTE: All typical values have been characterized but are not tested.

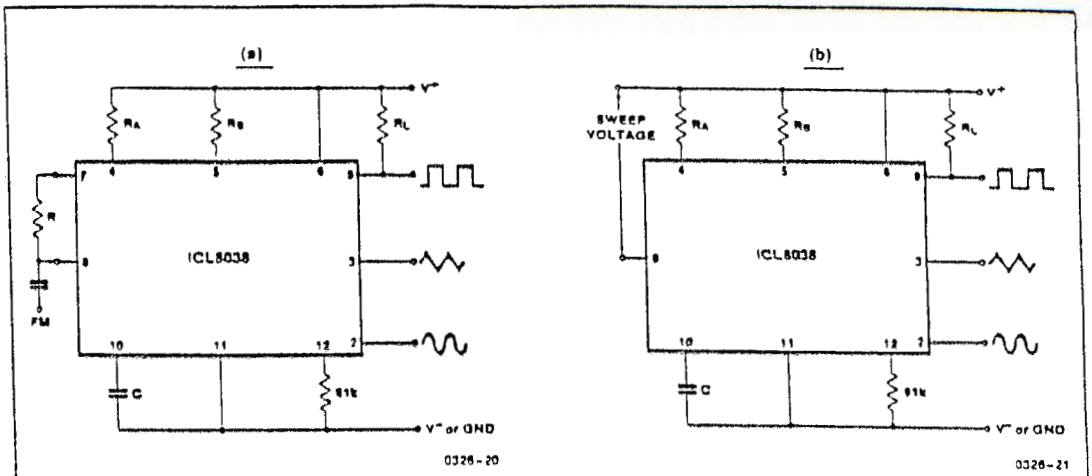


Figure 7: Connections for Frequency Modulation (a) and Sweep (b)

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 7a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 7b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at $V_{sweep} = 0$). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by ($\frac{1}{3}$ V_{SUPPLY} − 2V).

APPLICATIONS

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 8 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 9 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred millivolts. The Circuit of Figure 10 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

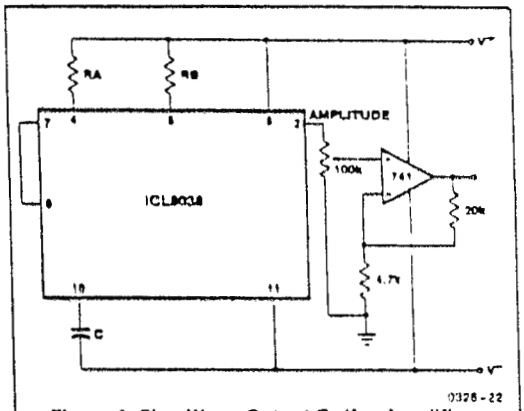


Figure 8: Sine Wave Output Buffer Amplifiers

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 11.

USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop as shown in Figure 12. In this application the remaining functional blocks, the

NOTE: All typical values have been characterized but are not tested.

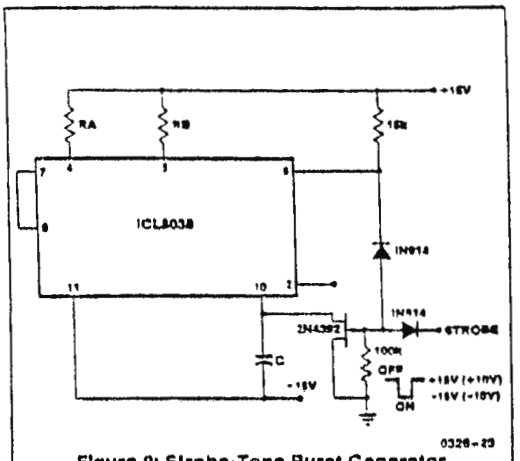


Figure 9: Strobe-Tone Burst Generator

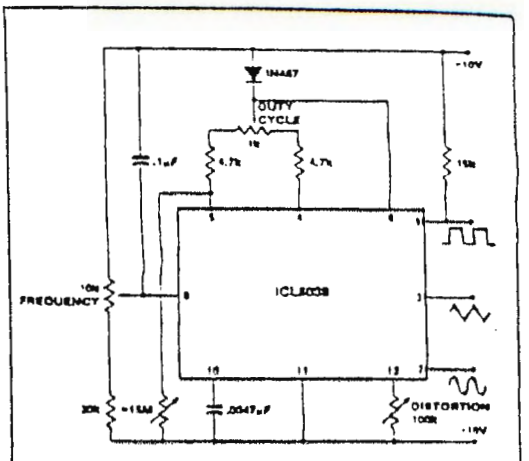


Figure 10: Variable Audio Oscillator, 20Hz to 20kHz

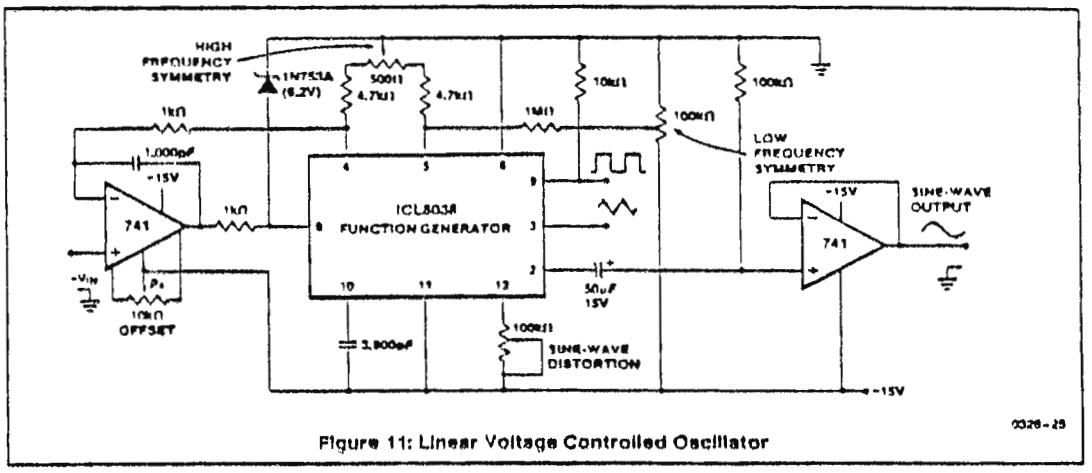


Figure 11: Linear Voltage Controlled Oscillator

phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC4344, NE562, HA2800, HA2820)

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note A013, "Everything You Always Wanted to Know About The ICL8038."

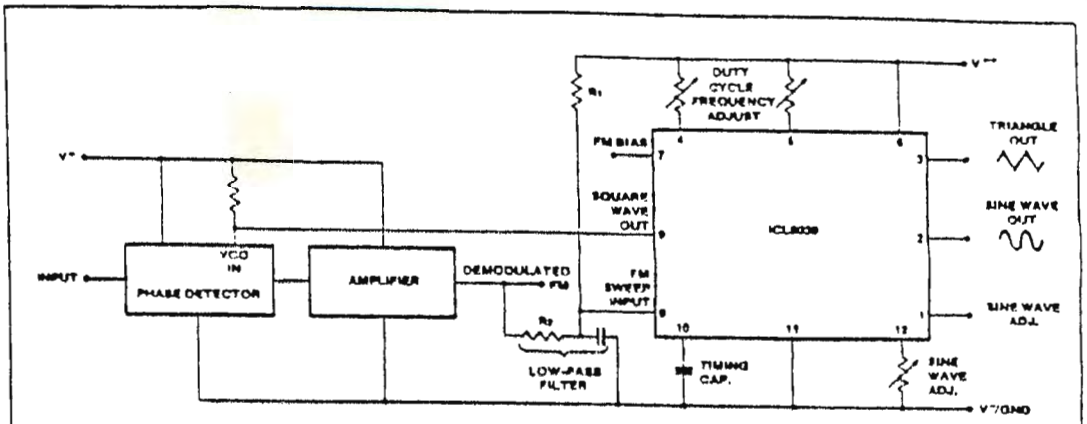


Figure 12: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

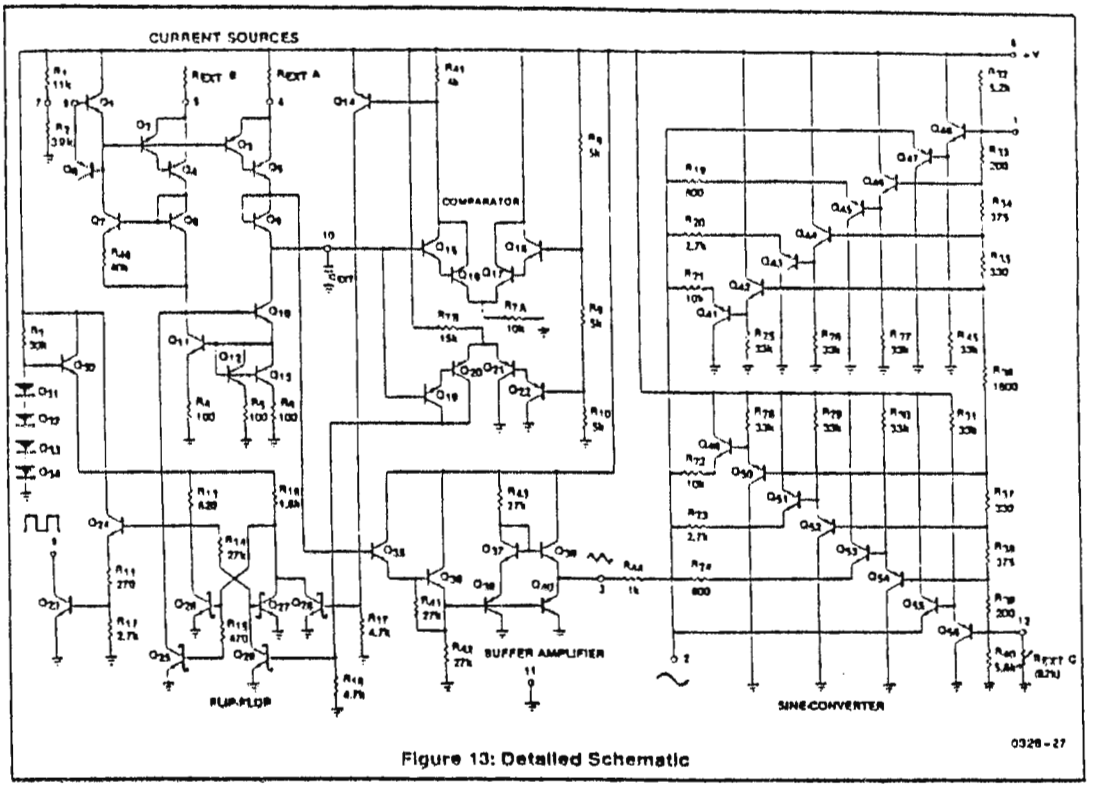


Figure 13: Detailed Schematic

NOTE: All typical values have been characterized but are not tested.

MOTOROLA

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input Nor Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B
8-Input NOR Gate

MC14081B
Quad 2-Input AND Gate

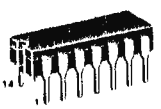
MC14082B
Dual 4-Input AND Gate

6

B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices (Exceptions: MC14068B and MC14078B)



L SUFFIX
CERAMIC
CASE 632

P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

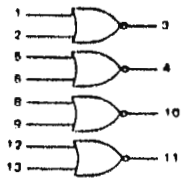
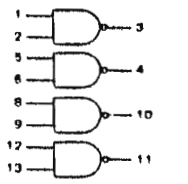
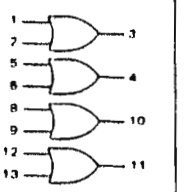
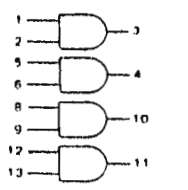
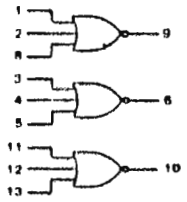
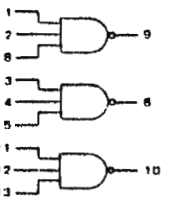
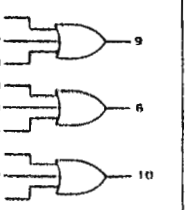
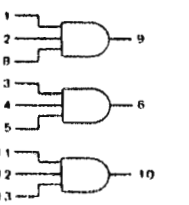
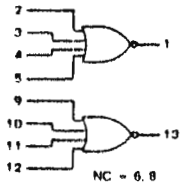
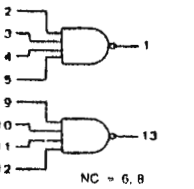
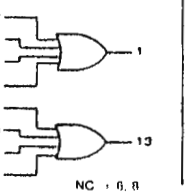
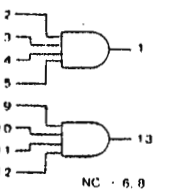
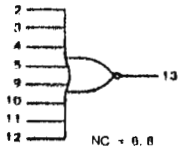
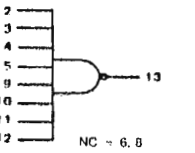
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

CMOS B-SERIES GATES

LOGIC DIAGRAMS

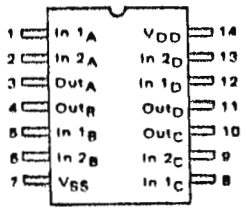
	NOR	NAND	OR	AND
2 INPUT	MC14001B Quad 2-Input NOR Gate	MC14011B Quad 2-Input NAND Gate	MC14071B Quad 2-Input OR Gate	MC14081B Quad 2-Input AND Gate
				
3 INPUT	MC14025B Triple 3-Input NOR Gate	MC14023B Triple 3-Input NAND Gate	MC14075B Triple 3-Input OR Gate	MC14073B Triple 3-Input AND Gate
				
4 INPUT	MC14002B Dual 4-Input NOR Gate	MC14012B Dual 4-Input NAND Gate	MC14072B Dual 4-Input OR Gate	MC14082B Dual 4-Input AND Gate
	 NC = 6, 8	 NC = 6, 8	 NC = 6, 8	 NC = 6, 8
8 INPUT	MC14078B 8-Input NOR Gate	MC14068B 8-Input NAND Gate		
	 NC = 6, 8	 NC = 6, 8		

V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

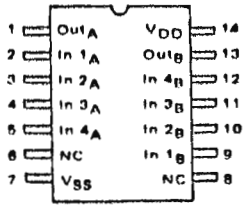
CMOS B-SERIES GATES

PIN ASSIGNMENTS

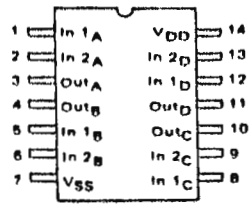
MC14001B
Quad 2-Input NOR Gate



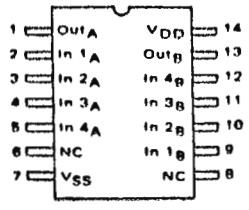
MC14002B
Dual 4-Input NOR Gate



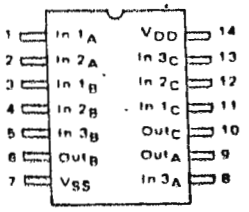
MC14011B
Quad 2-Input NAND Gate



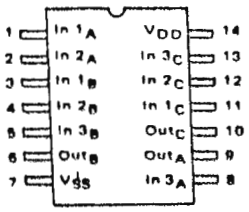
MC14012B
Dual 4-Input NAND Gate



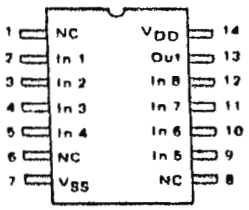
MC14023B
Triple 3-Input NAND Gate



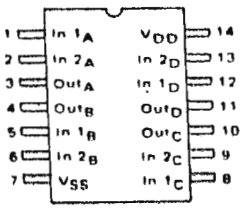
MC14025B
Triple 3-Input NOR Gate



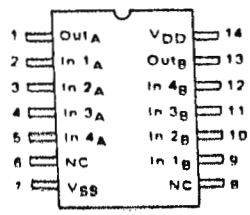
MC14068B
8-Input NAND Gate



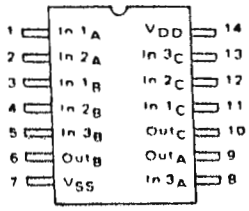
MC14071B
Quad 2-Input OR Gate



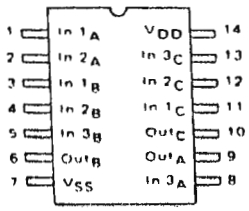
MC14072B
Dual 4-Input OR Gate



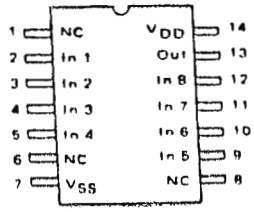
MC14073B
Triple 3-Input AND Gate



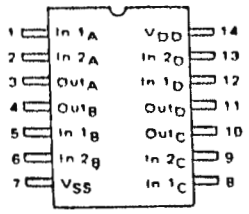
MC14075B
Triple 3-Input OR Gate



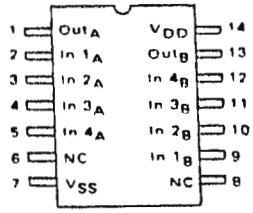
MC14078B
8-Input NOR Gate



MC14081B
Quad 2-Input AND Gate



MC14082B
Dual 4-Input AND Gate



NC = No Connection

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/N							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}/N							
		15	I_T = (0.9 μA/kHz) f + I_{DD}/N							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

B-SERIES GATE SWITCHING TIMES

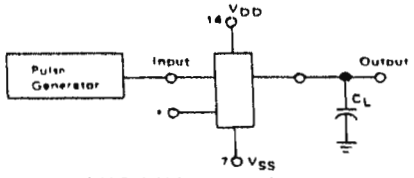
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC140018, MC14011B only						
t_{PLH}, t_{PHL} = (0.80 ns/pF) C_L + 80 ns		5.0	—	175	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	—	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	—	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	—	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	—	50	100	
8 Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	—	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	—	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	—	60	110	

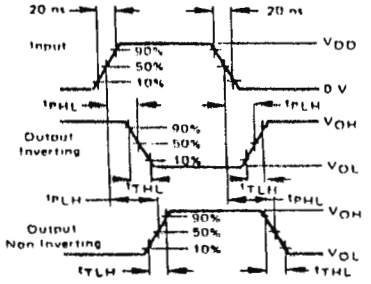
*The formulas given are for the typical characteristics only at 25°C

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.



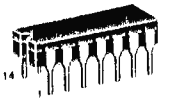
MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

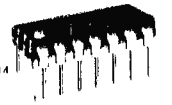
The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON}, Use The HC4066 High-Speed CMOS Device



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

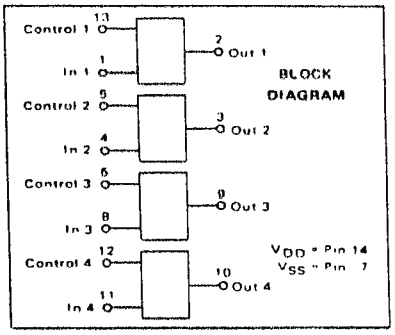
MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = −55° to 125°C for all packages

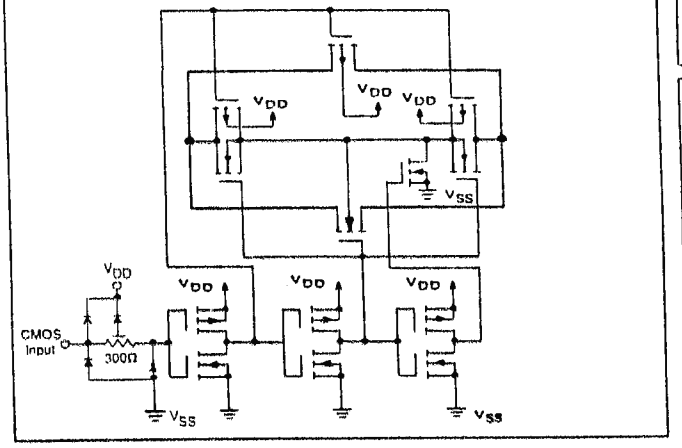
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

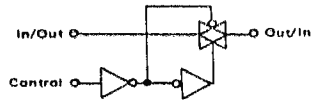
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C



CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}. Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV**	— — —	0.25 0.5 1.0	— — —	0.005 0.010 0.015	0.25 0.5 1.0	— — —	7.5 15 30	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	$T_A = 25°C$ only The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz)f + I_{DD} (0.20 μA/kHz)f + I_{DD} (0.36 μA/kHz)f + I_{DD}				μA
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	$V_{in} = 0$ V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV**, $V_{in} = V_{IL}$ or V_{IH} (Control), and $V_{in} = 0$ to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	— —		—	—	—	0.47	—	—	—	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

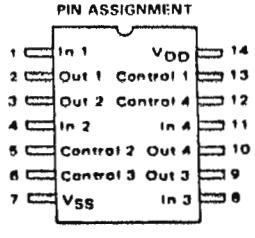
ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Times (V_{SS} = 0 Vdc)						
Input to Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns		5.0	—	20	40	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns		10	—	10	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		15	—	7.0	15	
Control to Output (R_L = 1 kΩ) (Figure 2)						
Output "1" to High Impedance	t_{PHZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
Output "0" to High Impedance	t_{PLZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
High Impedance to Output "1"	t_{PZH}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
High Impedance to Output "0"	t_{PZL}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
Second Harmonic Distortion (V_{SS} = −5 Vdc) (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) (V_{SS} = −5 Vdc) (R_L = 1 kΩ, 20 Log $\frac{V_{out}}{V_{in}}$ = −3 dB, C_L = 50 pF, V_{in} = 5 V_{p-p})	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) (V_{SS} = −5 Vdc) (V_{in} = 5 V_{p-p}, R_L = 1 kΩ, f_{in} = 1.0 MHz) (Figure 3)	—	5.0	—	−50	—	dB
Channel Separation (Figure 4) (V_{SS} = −5 Vdc) (V_{in} = 5 V_{p-p}, R_L = 1 kΩ, f_{in} = 8.0 MHz) (Switch A ON, Switch B OFF)	—	5.0	—	−50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) (V_{SS} = −5 Vdc) (R_1 = 1 kΩ, R_L = 10 kΩ, Control t_{TLH} = t_{THL} = 20 ns)	—	5.0	—	300	—	mV_{p-p}

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



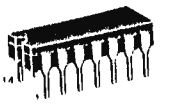
MC14068B
See Page 6-5

MC14069UB

HEX INVERTER

The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperatur Range
- Triple Diode Protection on All Inputs (see Page 5-2)
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications



L SUFFIX
CERAMIC
CASE 632

P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXUBCP Plastic
MC14XXXUBCL Ceramic
MC14XXXUBD SOIC

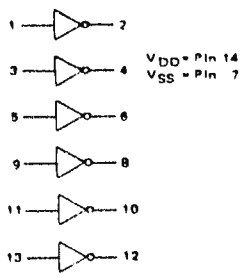
T_A = −55° to 125°C for all packages

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

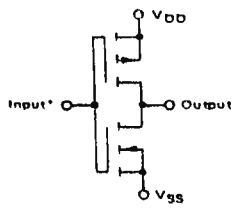
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM



CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



*Double diode protection on all inputs not shown.

PIN ASSIGNMENT

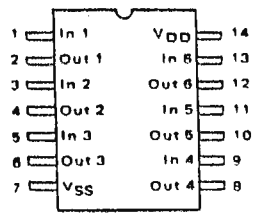
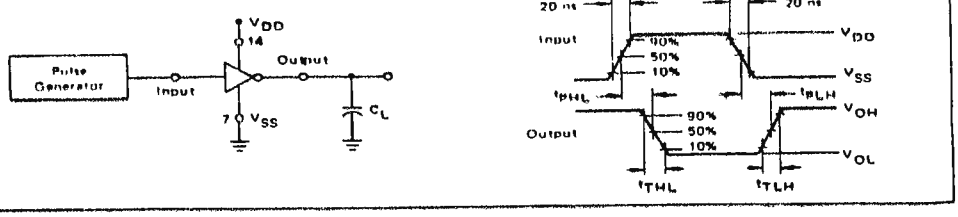


FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD}	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 Vdc)	V_{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
(V_O = 9.0 Vdc)		10	—	2.0	—	4.50	2.0	—	2.0	
(V_O = 13.5 Vdc)		15	—	2.5	—	6.75	2.5	—	2.5	
"1" Level (V_O = 0.5 Vdc)	V_{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
(V_O = 1.0 Vdc)		10	8.0	—	8.0	5.50	—	8.0	—	
(V_O = 1.5 Vdc)		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/6							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}/6							
		15	I_T = (0.9 μA/kHz) f + I_{DD}/6							
Output Rise and Fall Times** (C_L = 50 pF) t_{TLH},t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{TLH},t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{TLH},t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	5.0	—	—	—	100	200	—	—	ns
		10	—	—	—	50	100	—	—	
		15	—	—	—	40	80	—	—	
Propagation Delay Times** (C_L = 50 pF) t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 20 ns t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 22 ns t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 17 ns	t_{PLH}, t_{PHL}	5.0	—	—	—	65	125	—	—	ns
		10	—	—	—	40	75	—	—	
		15	—	—	—	30	55	—	—	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MC14174B

HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Functional Equivalent to TTL 74174

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = −55 to 125°C for all packages

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

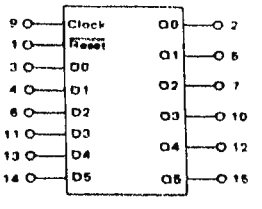
TRUTH TABLE
(Positive Logic)

INPUTS			OUTPUT	
Clock	Data	Reset	Q	
↑	0	1	0	
↑	1	1	1	
↓	X	1	Q	No Change
X	X	0	0	

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.1 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.3 μA/kHz) f + I_{DD}							
		15	I_T = (3.7 μA/kHz) f + I_{DD}							

6

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

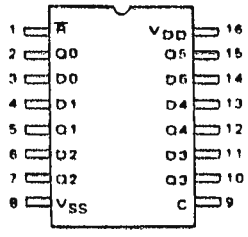
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ #	All Types Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time — Clock to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 165 ns		5.0	—	210	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 64 ns		10	—	85	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 52 ns		15	—	65	120	
Propagation Delay Time — $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 205 ns		5.0	—	250	500	
t_{PHL} = (0.36 ns/pF) C_L + 79 ns		10	—	100	200	
t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	—	75	150	
Clock Pulse Width	t_{WH}	5.0	150	75	—	ns
		10	90	45	—	
		15	70	35	—	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	
Clock Pulse Frequency	f_{cl}	5.0	—	7.0	2.0	MHz
		10	—	12.0	5.0	
		15	—	15.5	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	μs
		10	—	—	5.0	
		15	—	—	4.0	
Data Setup Time	t_{su}	5.0	40	20	—	ns
		10	20	10	—	
		15	15	0	—	
Data Hold Time	t_h	5.0	80	40	—	ns
		10	40	20	—	
		15	30	15	—	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	250	125	—	ns
		10	100	50	—	
		15	80	40	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT



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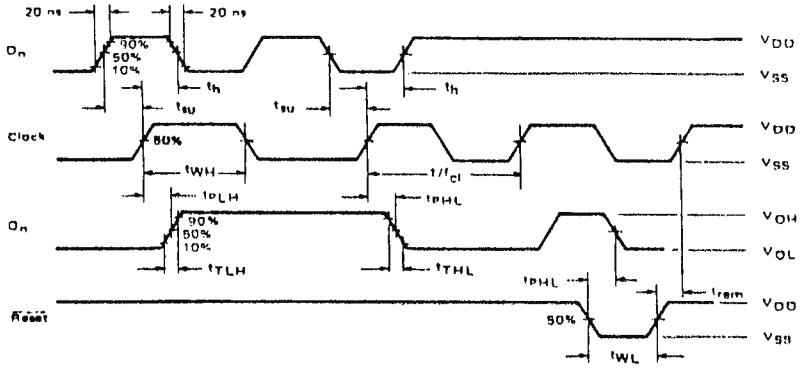
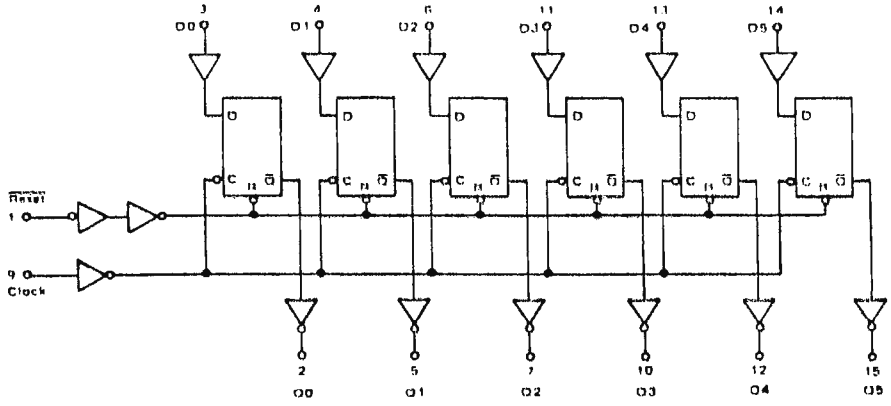
TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MC14518B
MC14520B

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

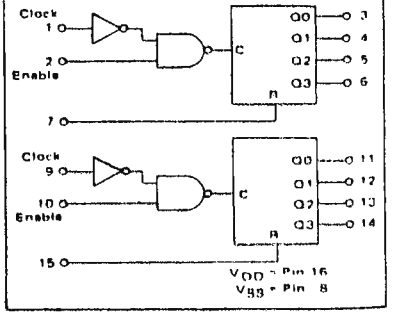
T_A = −55 to 125°C for all packages

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM



TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

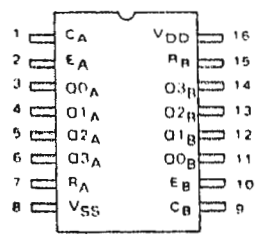
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002

PIN ASSIGNMENT



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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

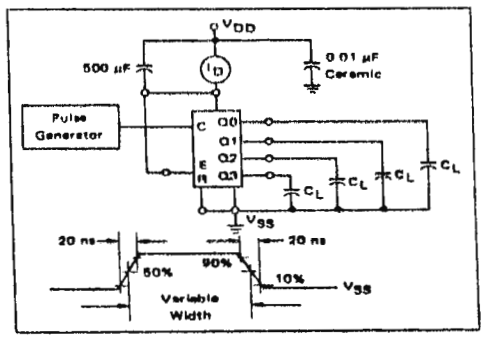
Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q/Enable to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
Reset to Q	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	330	660	
t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	130	230	
t_{PHL} = (0.55 ns/pF) C_L + 95 ns		15	–	90	170	
Clock Pulse Width	$t_{w(H)}$, $t_{w(L)}$	5.0	200	100	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	–	–	15	µs
		10	–	–	5	
		15	–	–	4	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	–	ns
		10	200	100	–	
		15	140	70	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	280	145	–	ns
		10	120	55	–	
		15	90	40	–	
Reset Removal Time	t_{rem}	5.0	-5	-45	–	ns
		10	15	-15	–	
		15	20	-5	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14555B
MC14556B

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary to hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = −55 to 125°C for all packages

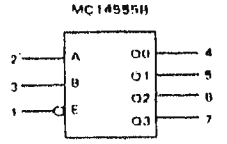
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

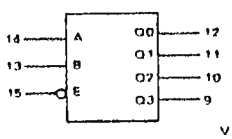
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

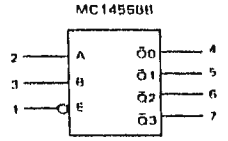
BLOCK DIAGRAM

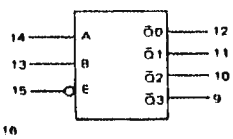
MC14555B





MC14556B





V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT									
E	B	A	Q3	Q2	Q1	Q0	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.85 μA/kHz) f + I_{DD} I_T = (1.70 μA/kHz) f + I_{DD} I_T = (2.60 μA/kHz) f + I_{DD}							μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

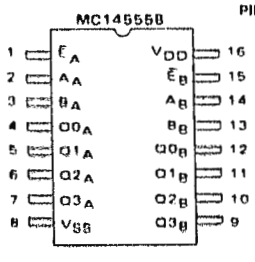
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

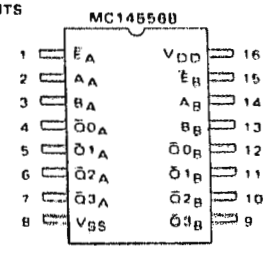
where I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002

PIN ASSIGNMENTS

MC14555B



MC14556B



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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time — A, B to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	—	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	—	95	190	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	—	70	140	
Propagation Delay Time — E to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	—	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	—	85	170	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	—	65	130	

*The formulas given are for the typical characteristics only at 25°C

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

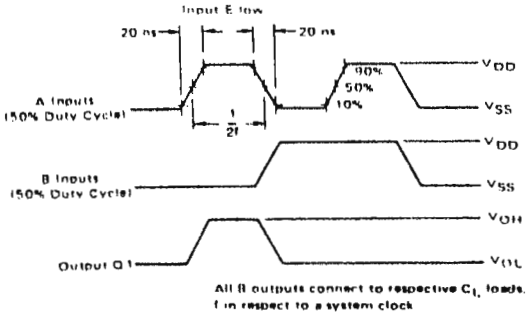
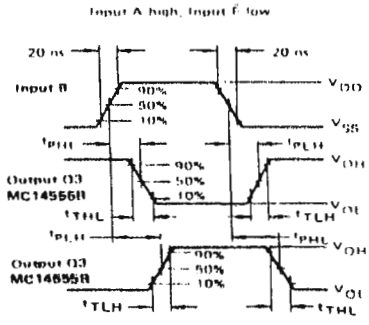
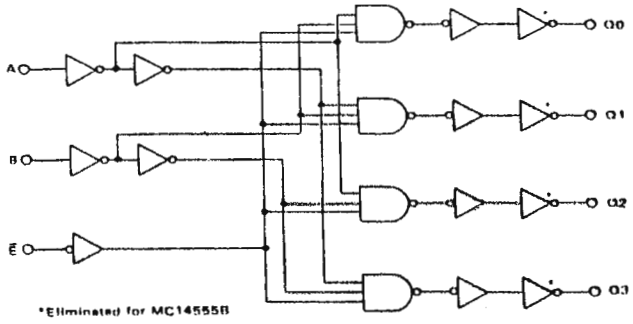


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



6

LOGIC DIAGRAM
(1/2 of Dual)



National Semiconductor

LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

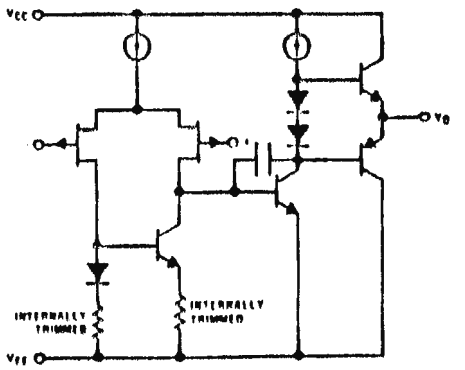
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	5 mV max
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	15 V/μs
■ Low supply current	7.2 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz – 20 kHz	< 0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Simplified Schematic

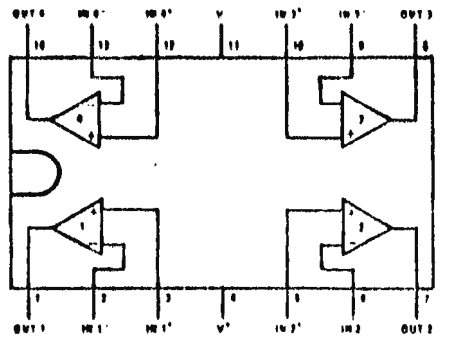
¼ Quad



TL/H/5647–13

Connection Diagram

Dual-In-Line Package



TL/H/5647–1

Top View

Order Number LF147J, LF347M, LF347BN, LF347N, LF147J/883 or LF147J/883*
See NS Package Number D14E, J14A, M14A or N14A

*Available per SMD #8102306, JM38510/11906

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	± 22V	± 18V
Differential Input Voltage	± 38V	± 30V
Input Voltage Range (Note 1)	± 19V	± 15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Power Dissipation (Notes 3 and 9)	800 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}		
Cavity DIP (D) Package		80°C/W
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

	LF147	LF347B/LF347
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) 900V

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$		1	5		3	5		5	10	mV
		Over Temperature			6			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$	50	100		50	100		25	100		V/mV
		$V_O = \pm 10V$, $R_L = 2\ k\Omega$										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	± 12	± 13.5		± 12	± 13.5		± 12	± 13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	± 11	+ 15 − 12		± 11	+ 15 − 12		± 11	+ 15 12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz – 20 kHz (Input Referred)		120			120			120		dB
SR	Slew Rate	V_S = ± 15V, T_A = 25°C	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	V_S = ± 15V, T_A = 25°C	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		20			20			20		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_J = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}

Note 4: The LF147 is available in the military temperature range −55°C ≤ T_A ≤ 125°C, while the LF347B and the LF347 are available in the commercial temperature range 0°C ≤ T_A ≤ 70°C. Junction temperature can rise to T_J max = 150°C

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for V_S = ± 20V for the LF147 and for V_S = ± 15V for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_J = T_A + θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ± 5V to ± 15V for the LF347 and LF347B and from V_S = ± 20V to ± 5V for the LF147

Note 8: Refer to RETS147X for LF147D and LF147J military specifications

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits

Note 10: Human body model, 1.5 kΩ in series with 100 pF

National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

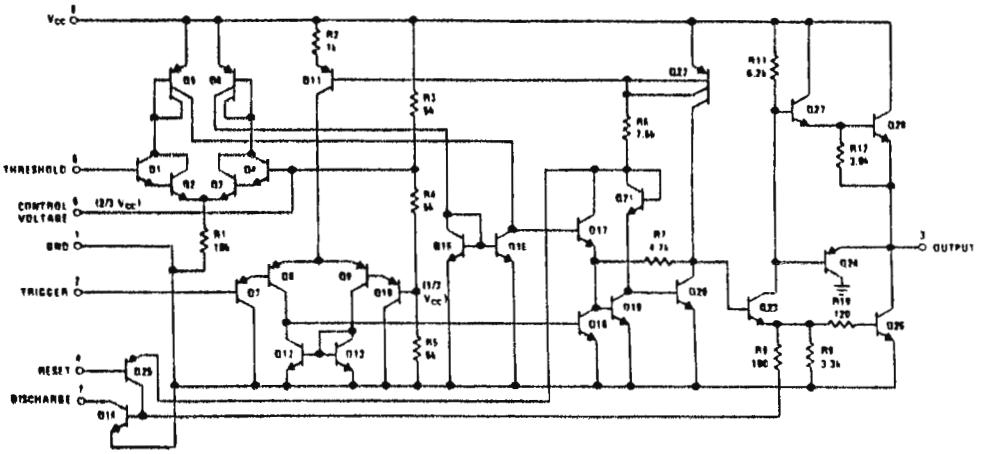
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage + 18V

Power Dissipation (Note 1)
- LM555H, LM555CH 760 mW
- LM555, LM555CN 1180 mW

Operating Temperature Ranges
- LM555C 0°C to + 70°C
- LM555 − 55°C to + 125°C

Storage Temperature Range − 65°C to + 150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 Seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 Seconds) 215°C
  - Infrared (15 Seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = + 5V to + 15V, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, (unless otherwise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15V$							
	$I_{SINK} = 10$ mA		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100$ mA		2	2.2		2	2.5	V
	$I_{SINK} = 200$ mA		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8$ mA		0.1	0.25				V
	$I_{SINK} = 5$ mA					0.25	0.35	V
Output Voltage Drop (High)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15V$		12.5			12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15V$	13	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°C/W (TO-5), 106°C/W (DIP) and 170°C/W (SO-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at $V_{CC} = 5V$.

Note 3: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$

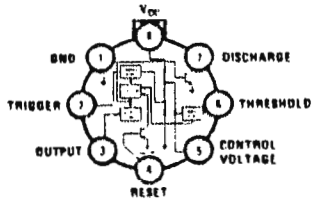
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package

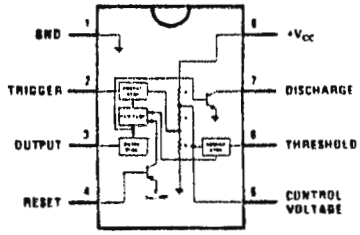


TL/H/7851–2

Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/7851–3

Top View

Order Number LM555J, LM555CJ, LM555CM or LM555CN
See NS Package Number J08A, M08A or N08E

National Semiconductor

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

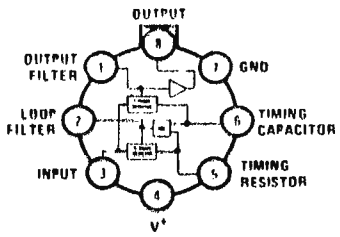
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

Metal Can Package

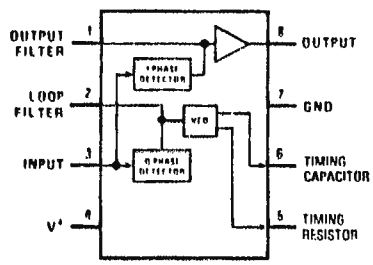


TL/H/6975–1

Top View

Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/6975–2

Top View

Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 1)	1100 mW
V_8	15V
V_3	−10V
V_2	V_4 + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM567H	−55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics AC Test Circuit, T_A = 25°C, V^+ = 5V

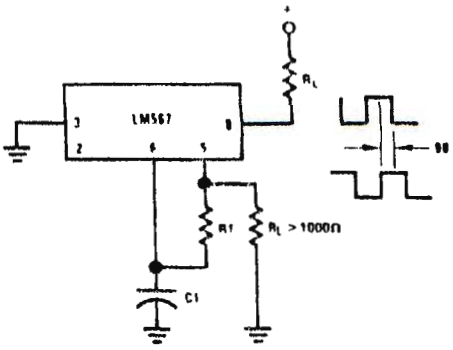
Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_c
Largest Detection Bandwidth Skew			1	2		2	3	% of f_c
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 − 6.75V		±1	±2		±1	±5	%/V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75−5.75V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ± 60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V − 6.75V 4.75V − 9V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 2: Refer to RETS567X drawing for specifications of military LM567H version.

Typical Applications (Continued)

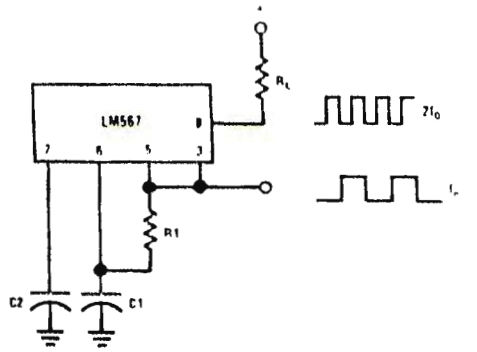
Oscillator with Quadrature Output



Connect Pin 3 to 2.8V to Invert Output

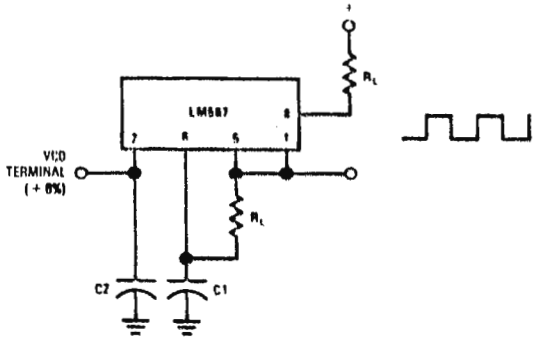
TL/H/6975–6

Oscillator with Double Frequency Output



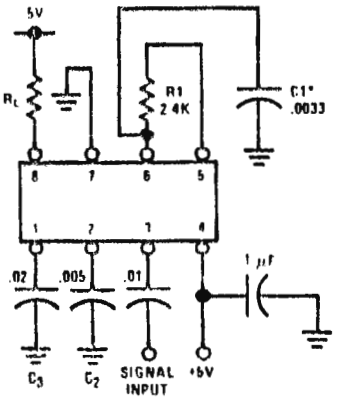
TL/H/6975–7

Precision Oscillator Drive 100 mA Loads



TL/H/6975–8

AC Test Circuit



TL/H/6975–9

f_o = 100 kHz + 6V

*Note: Adjust for f_o = 100 kHz

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \approx \frac{1}{1.1\,R_1C_1}$$

The bandwidth of the filter may be found from the approximation

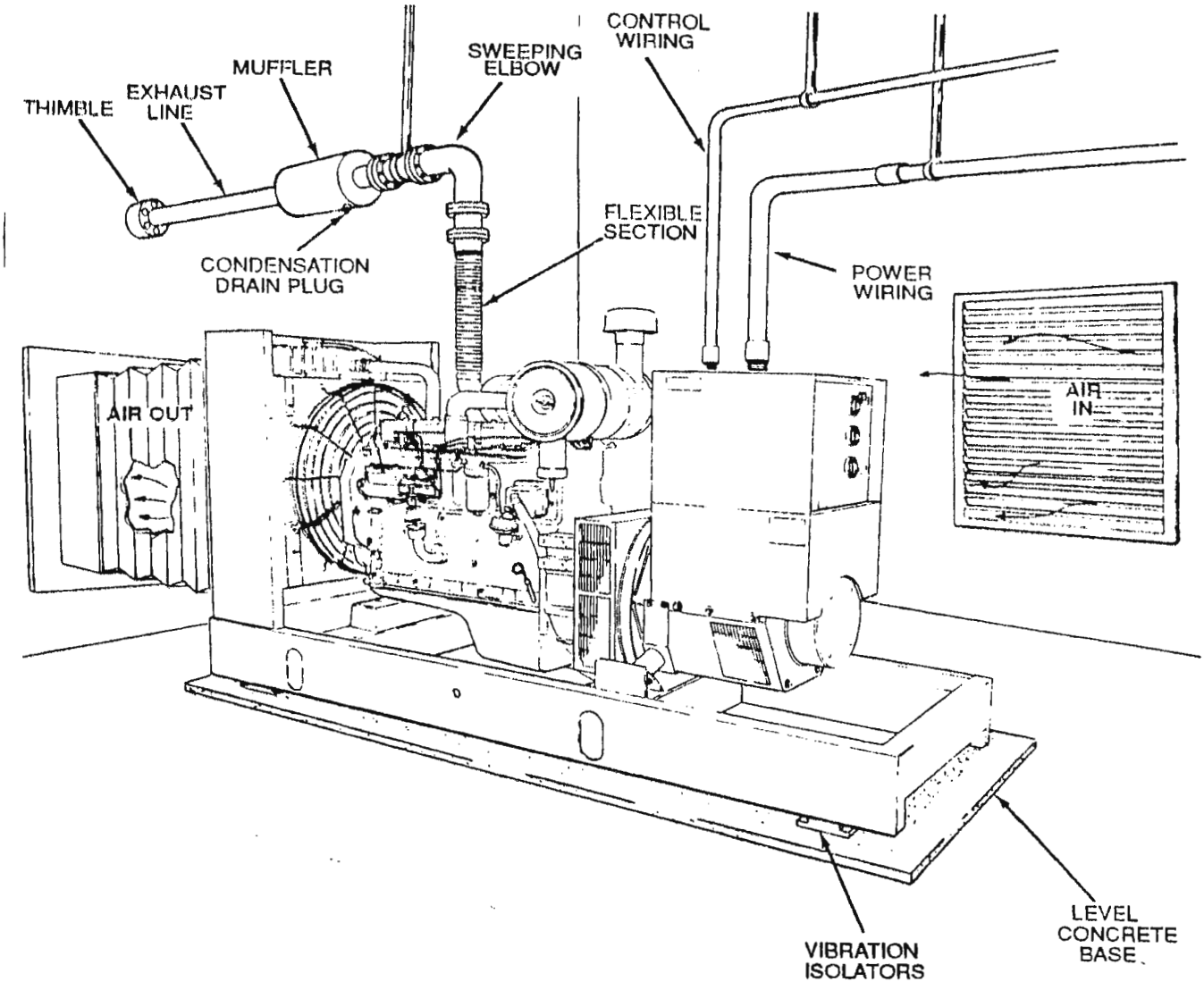
$$BW = 1070\sqrt{\frac{V_i}{f_oC_2}} \text{ in \% of } f_o$$

Where:

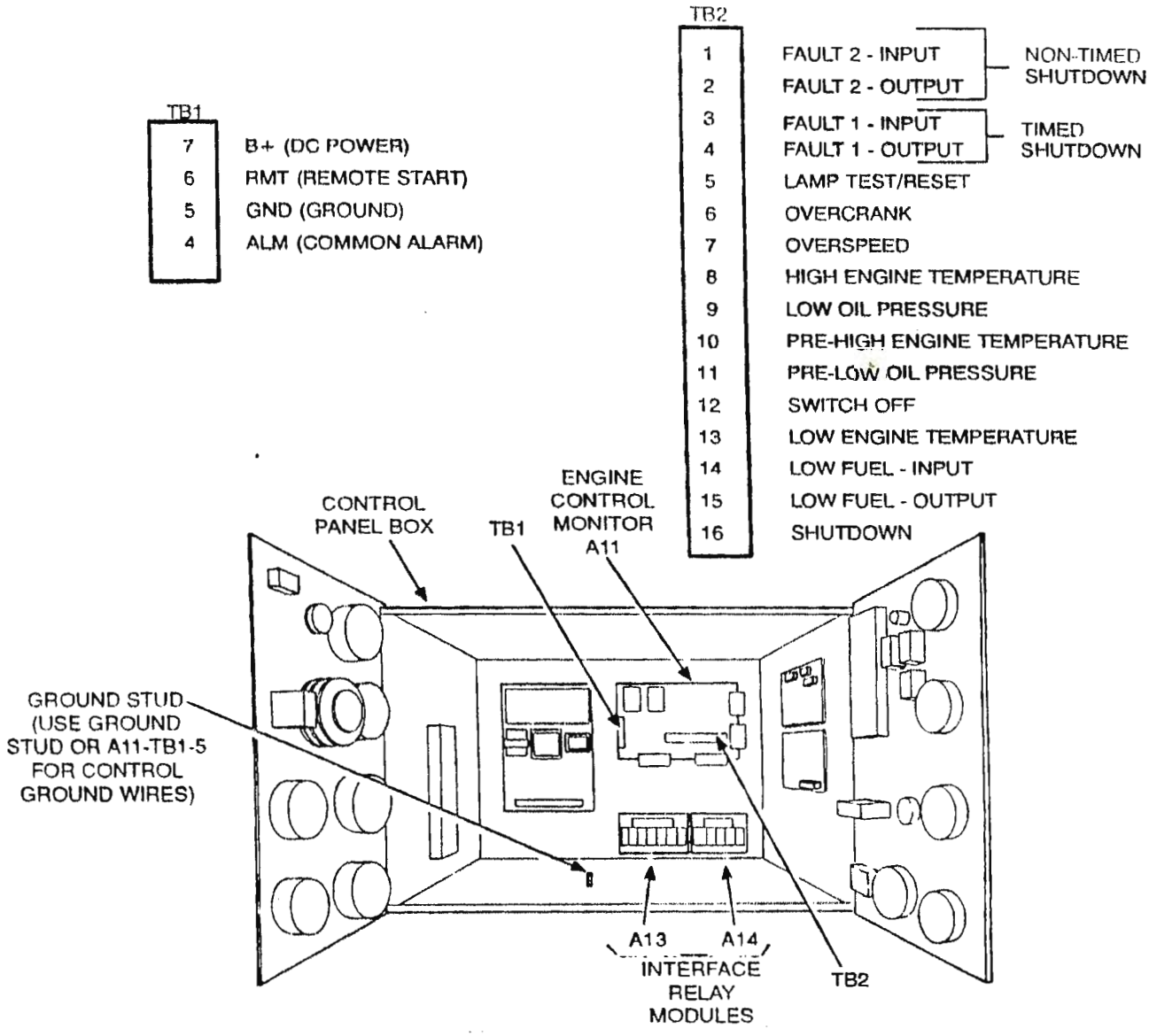
V_i = Input voltage (volts rms), $V_i \leq 200$ mV

C_2 = Capacitance at Pin 2 (μF)

Planta Eléctrica.



Vista Interior del Panel de Control.



FUEL SYSTEM

With the genset operating, inspect the fuel supply lines, filters and fittings for leaks. Check any flexible sections for cuts, cracks and abrasions and make sure they are not rubbing against anything that could cause breakage.

⚠WARNING ***Leaking fuel will create a fire hazard that can result in severe personal injury or death if ignited by a spark. If any leaks are detected, have them corrected immediately.***

DC ELECTRICAL SYSTEM

With the generator set off, check the terminals on the battery for clean and tight connections. Loose or corroded connections create resistance that can hinder starting. Clean and reconnect the battery cables if loose. Always connect the negative battery cable last.

⚠WARNING ***Ignition of explosive gases can cause explosion and fire, resulting in severe personal injury or death. Do not smoke while servicing the batteries.***

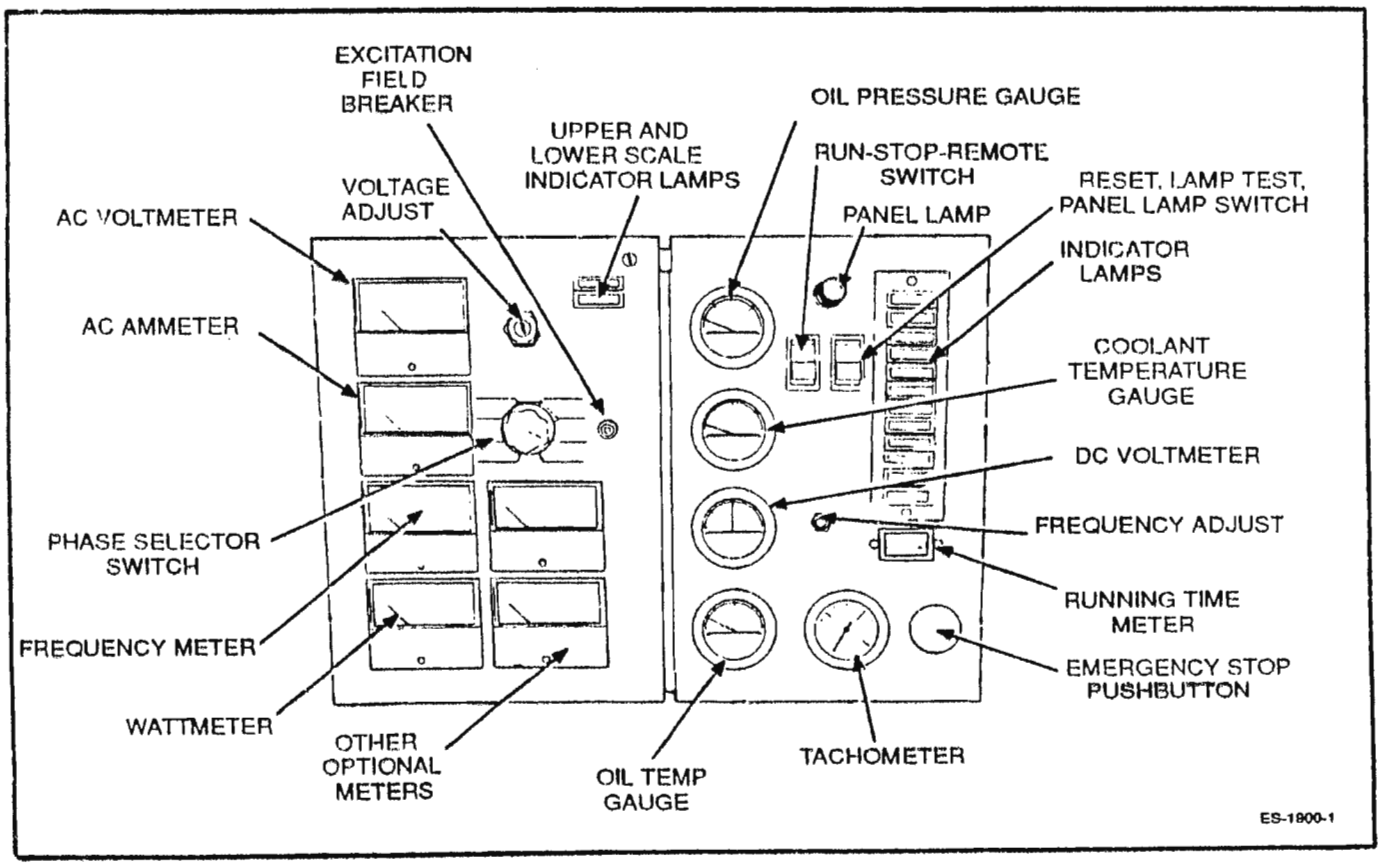
COOLING SYSTEM

When the engine is first started, remove the radiator pressure cap and monitor the coolant level. As trapped air is expelled from the system, the coolant level will drop and additional coolant must be added. Replace the pressure cap when the coolant level is stable.

MECHANICAL ADJUSTMENTS

With the generator stopped, check for loose belts and fittings, leaking gaskets and hoses, or any signs of mechanical damage. If any problems are found, have them corrected immediately.

With the set running, listen for any unusual noises that can indicate mechanical problems. Check the oil pressure frequently. Refer to Operator's or Service Manual for required adjustments.



CONTROL PANEL WITH OPTIONS

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- *Operator's Manual. Max Trac 888. Radio System. Movile Products Division. Motorola.*

- *Manual de Prácticas de Laboratorio. Modulaciones Analógicas e Impulsivas. Electrónica "Vennetta".*