"MONITOREO Y REGULACIÓN DE UN GENERADOR DE VOLTAJES POR TELECONTROL"

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INTRODUCCIÓN

El trabajo que se presenta a continuación, está orientado hacia la solución de un problema que se da en una planta industrial local, mediante la aplicación de un telemando por RF.

El sistema implementado es inalámbrico, pues este tipo de sistema permite una optimización de recursos, en cuanto a facilidad de transporte, independencia de operación, etc.

A partir de la visita a la empresa se pudo observar que la utilización de autómatas obliga a los encargados de mantenimiento a un proceso de calibrado y ajuste de parámetros en donde la distancia entre los puntos clave en ese proceso, hacen que la realización de éste sea tediosa, pues requiere que las operaciones sean realizadas por más de una persona o en su defecto, realizadas por una pero en un lapso de tiempo mucho mayor, lo cual da como resultado un incremento de costos para la empresa pues se atrasa la producción.

A partir de lo anterior, el sistema propuesto permite a un solo operario realizar las funciones de dos o más, lo cual hace más eficientes y rápidas las tareas de mantenimiento preventivo y correctivo en la planta reduciendo los costos de producción a partir del decremento del tiempo muerto de las máquinas.

Este beneficio que se obtiene, se hace más evidente al momento de controlar funciones, adquirir datos de éstas y tomar las decisiones u órdenes de actuación sobre el proceso, el cual dentro del mantenimiento industrial es de mucha utilidad debido a que se reduce el tiempo necesario para éste, debido a que se supera el obstáculo distancia.

Lo anterior permite una mayor eficiencia en la producción, a la vez que le da independencia al operador o encargado del mantenimiento de la máquina.

Ocasionalmente, es necesario realizar ajustes y mediciones en lugares de difícil acceso o incómodos, en donde el control y la medida a distancia son de gran utilidad, ya sea porque se necesite libertad de movimiento entre el punto de medida y el de recepción o porque en algunos casos el solo hecho de tratar de realizar una medición expone al operario a un riesgo físico, que solamente se puede evitar deteniendo el proceso de producción lo cual afecta en gran medida a la eficiencia buscada mediante un adecuado mantenimiento preventivo o correctivo.

Mediante el empleo de este sistema de telemando se persiguen los siguientes fines:

- La disminución de los gastos de operación.
- El aumento de la capacidad de producción de la planta.

Asimismo el sistema de telecontrol y telemedida implementado tiene las siguientes cualidades:

- Fiabilidad, es decir, el tipo de modulación es el menos propenso a ser afectado por ruido o interferencias típicas de un ambiente industrial.

- Agil, es decir, la velocidad de transmisión es la adecuada según la clase de información, elevada o discreta según las necesidades, ya que el tiempo que invierte la información para desplazarse es importante y de esto depende la rapidez en la que se tomarán las medidas o acciones pertinentes.

Basándose en lo anterior el sistema realiza básicamente dos tareas:

a) El envío de órdenes de control para gobernar los diferentes elementos del sistema a distancia, el cual es obtener un voltaje DC para que sea éste una simulación de la salida de un transductor.

b) La transmisión de la información correspondiente a la salida de voltaje, pues este dato de realimentación es de suma importancia para decidir sobre los estados de las diferentes magnitudes y/o parámetros del proceso.

OBJETIVOS

OBJETIVO GENERAL

Implementar un sistema de telecontrol capaz de regular una salida de voltaje usando como medio de transmisión radio frecuencias en el espacio abierto y en el cual simultáneamente se pueda leer dicho voltaje.

OBJETIVOS ESPECIFICOS

- Desarrollar un sistema que pueda reaccionar ante órdenes enviadas mediante RF.
- Implementar un conjunto de transmisores y receptores con un rango de operación de aproximadamente 20 metros.
- Diseñar un sistema de RF capaz de funcionar en un ambiente lleno de ruido, al cual deberá ser lo más insensible posible.

ALCANCES

- El sistema es de un tamaño que le permita ser portátil, para que su uso y manipulación sean cómodos al operario.

- El conjunto de transmisores y receptores permiten una comunicación simultánea entre el cuarto de control y el punto de regulación del voltaje.

- El voltaje generado es lo más estable posible, con una magnitud de hasta 12 voltios y una corriente máxima de 83.33 mA.

- El sistema implementado puede ser utilizado para otras aplicaciones de control a distancia como alarmas, control de iluminación, etc.

- Los pasos de control generan una resolución de aproximadamente 0.05 voltios

LIMITACIONES

- El ancho de banda de los convertidores no se puede exceder de los 12 kHz sin perder linealidad en la conversión de voltaje a frecuencia y viceversa.

METODOLOGIA DE LA INVESTIGACIÓN

La metodología se basó en tres etapas:

a) Investigación bibliográfica

b) Diseño

c) Implementación y pruebas de funcionamiento

La investigación bibliográfica se llevó a cabo mediante consulta en libros, revistas, exploración en Internet y se complementó con entrevistas a personas afines al campo de aplicación.

Todo lo anterior se hizo con énfasis en la obtención de los datos y conocimientos relacionados con telecontrol, telemedida y tratamientos de las señales electromagnéticas.

El diseño se utilizó como complemento a elementos ya existentes como en el caso de los transmisores, receptores y codificadores, los cuales son integrados de manera que al final el producto cumple con las metas o alcances propuestos.

La implementación se dividió en dos partes:

a) Implementación en breadboard

b) Fabricación del circuito impreso.

La primera parte en la implementación tuvo como objetivo el desarrollo del proyecto, depuración de fallas y ajustes necesarios para la optimización de recursos.

La segunda parte se orientó a darle un aspecto más funcional en cuanto a tamaño y desempeño. Esto último es de vital importancia, pues la implementación de este tipo de sistemas en circuitos impresos requiere de consideraciones y cuidados especiales.

DESCRIPCIÓN DEL PROYECTO

Dentro de una planta industrial de producción de detergente, se encuentra una sección destinada a la dosificación de diferentes sustancias (fragancia, colorantes, etc.), ésta se realiza a través de una banda transportadora del producto, en la cual la velocidad de la banda es inversamente proporcional al peso que lleva, esto es así para una adecuada dosificación.

El autómata gobierna todos los procesos de dosificación de acuerdo a un programa particular para cada producto o diferente marca de detergente.

En los cambios de parámetros, en las fallas de alimentación o en cualquier otro problema, entra en acción un plan de mantenimiento preventivo o correctivo.

En el proceso de mantenimiento de los autómatas en cuestión, se necesita generar un voltaje DC, para efectos de simular un voltaje de salida proveniente de un transductor, el cual hace la conversión del peso de la banda de transporte en voltaje, para que sea monitoreado por el autómata a través de una sonda conectada al transductor.

El trabajo del equipo de telecontrol es generar ese voltaje, visualizar su magnitud en el punto de mando para hacer las correcciones o ajustes necesarios en el cuarto de control de los autómatas, sin necesidad de estar en movimiento entre el punto de simulación y el cuarto de control.

En la actualidad este proceso no puede ser realizado por una persona, pues se encuentra con serios problemas en cuanto a movilización y tiempo, por lo cual es necesario que a menudo ésta solicite ayuda a otros operarios, llevando problemas secundarios a éstos, pues interrumpen sus labores para prestar su ayuda, eso si hay alguien disponible que pueda prestar dicha ayuda.

El equipo de telecontrol consta de dos elementos, uno donde se encontraría la pantalla y los controles y el otro donde se hallaría el generador de voltaje.

Cabe mencionar que este equipo no sólo es de utilidad en la planta de detergente, pues en las otras plantas aledañas donde se producen consomés, sazonadores, etc. se practica el mismo tipo de mantenimiento.

El sistema en general se puede dividir en dos etapas principales:

1) La generación de órdenes y punto de monitoreo o visualización del evento controlado.
2) La generación de voltaje (simulación).

La etapa 1 la forman los siguientes conjuntos:

a) Un transmisor de tonos.
b) Un receptor de frecuencias.
c) Un presentador LCD de 4 dígitos con resolución de 0.1 y luz posterior

La etapa 2 la forman los siguientes conjuntos:

a) Un receptor de tonos
b) Un contador descendente y ascendente de 8 bits.
c) Un convertidor digital-análogo.
d) Un transmisor de frecuencias.

ETAPA 1

TRANSMISOR DE TONOS

En el transmisor de tonos se encuentran dos osciladores/temporizadores (LM555) los cuales generan una frecuencia de 716.41 Hz que es utilizada para el incremento del voltaje de salida y otra de 1,142.86 Hz la cual es utilizada para el decremento. Los temporizadores están en modo astable y la frecuencia de oscilación es determinada por la siguiente fórmula:

$$f = \frac{1}{(RA + 2RB)C}$$

RA y RB son las resistencias de carga del capacitor C y RB es la responsable de la descarga del mismo.

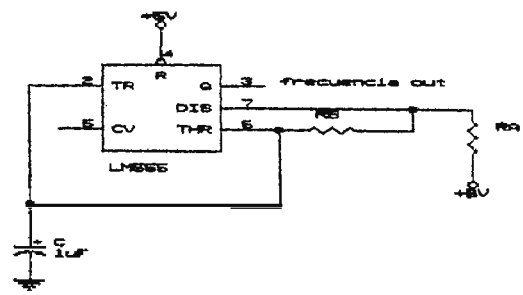


FIGURA 1

OSCILADOR LM555

Como se utiliza una combinación de dos resistencias para lograr los tiempos en alto y en bajo no se puede lograr obtener una señal cuadrada con semiciclos iguales. Los tiempos en alto y bajo se calculan de la siguiente manera, respectivamente:

$t1 = 0.693(RA + RB)C$

$t2 = 0.693 * RB * C$

Estas frecuencias son conmutadas hacia el transmisor (TX1) mediante los pulsadores que corresponden a la orden de ascenso o descenso, la cual es radiada en el espacio libre y modulada en frecuencia.

RECEPTOR DE FRECUENCIAS

El conjunto del receptor de RF lo constituyen *tres dispositivos*:

1) *Filtro Sallen y Key*

2) Comparador de nivel

3) Convertidor de Frecuencia a Voltaje

El receptor de RF obtiene a su entrada una señal de pulsos cuadrados provenientes del receptor (RX2). La señal es filtrada con una frecuencia de corte 9,947.18 Hz mediante un filtro pasa bajos del tipo Sallen y Key de segundo orden para de esa manera eliminar interferencias causadas por estaciones de radiodifusión. El par de resistencias y de capacitores de igual valor son los responsables de la frecuencia de corte; la cual se calcula de la siguiente forma:

$$f = \frac{1}{2\pi RC}$$

Las resistencias R7 y R6 definen la ganancia la que en este caso es de 0.5.

$$Ganancia = -\frac{R7}{R8}$$

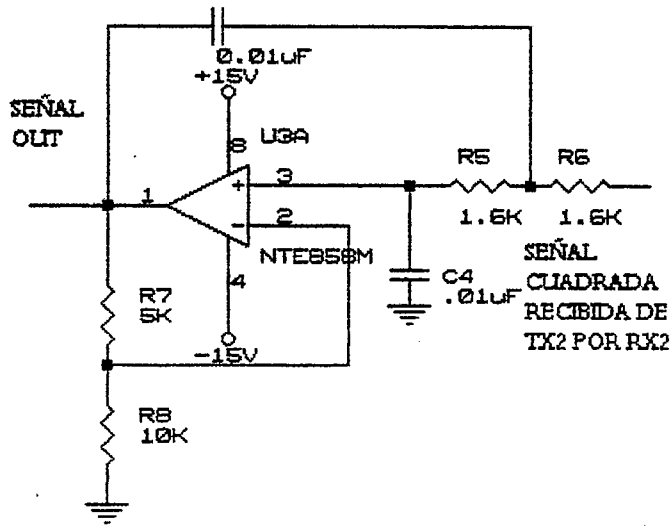


FIGURA 2

FILTRO SALLEN Y KEY

Una vez filtrada se compara esta señal mediante el amplificador operacional (NTE858) para nuevamente adecuar los pulsos hacia la forma cuadrada para después ser convertida de frecuencia a voltaje por el convertidor de frecuencia a voltaje (LM331). El comparador de nivel tiene una referencia en la entrada inversora variable, para ajustar el nivel adecuado de comparación debido a que a veces se dan atenuaciones en la señal al momento de ser transmitidas, obteniéndose en la salida una señal de pulsos cuadrados con una amplitud de 5V.

El convertidor de frecuencia a voltaje necesita en su entrada una señal cuadrada de más de 3V de amplitud. El LM331 detecta un cambio en la señal de entrada cuando el voltaje del pin 6 es inferior al voltaje en el pin 7 produciendo que se fije un latch interno e inicie una temporización durante la cual proporciona una corriente en el pin 1 igual al Vref/(POT1+R3) por un tiempo t=1.1R4C3; el capacitor C2 filtra las pulsaciones de corriente del pin 1 y la corriente promedia pasa a través de R2. El voltaje de R2 es el nivel de voltaje correspondiente a la frecuencia de la señal de entrada.

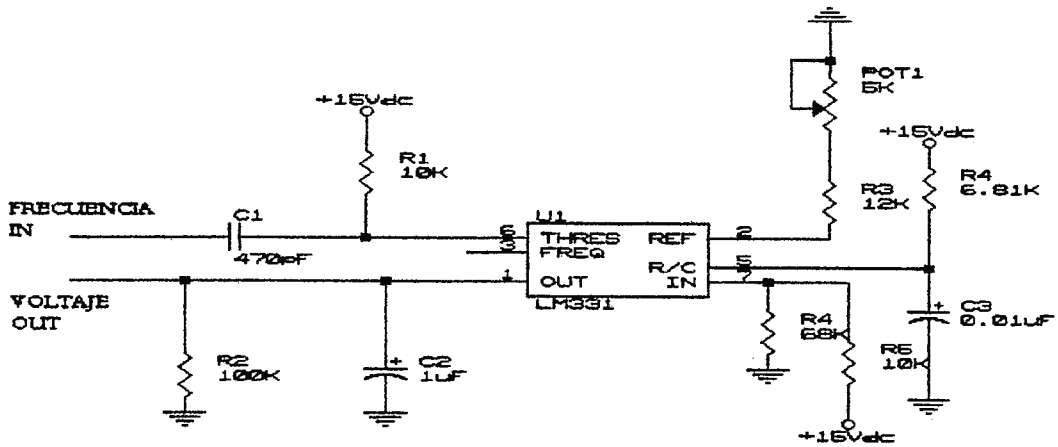


FIGURA 3

CONVERTIDOR DE FRECUENCIA A VOLTAJE

Este voltaje es introducido en el presentador de cristal líquido de 3.5 con luz posterior (PM-188BL), el cual tiene de forma integrada el convertidor de voltaje análogo a digital y el manejador de los segmentos.

ETAPA 2

RECEPTOR DE TONOS

Las ordenes transmitidas por TX1 son recibidas en RX1, estas señales captadas por el receptor de FM (RX1) son inyectadas hacia los detectores de tono (LM567) los cuales mantienen una salida en alto (+5V) hasta que se detecte la frecuencia para la que han sido diseñados, posterior a esto se genera un cambio de nivel en la salida y pasa a ser un bajo (0V) lo cual polariza el LED y este enciende dando por confirmado el enganche del tono. La frecuencia de enganche de los dos LM567 es determinada por R y C del diagrama.

$$f = \frac{1}{1.1RC}$$

Los capacitores en los pines 1 y 2 son los responsables del ancho de banda de detección. El capacitor del pin 1 se mantiene fijo y se regula el del pin 2 para ajustar el ancho de banda. La ecuación del ancho de banda es:

$$BW = 1070\sqrt{\frac{Vi}{fC2}}$$

Donde, Vi es el voltaje de entrada y f la frecuencia de enganche.

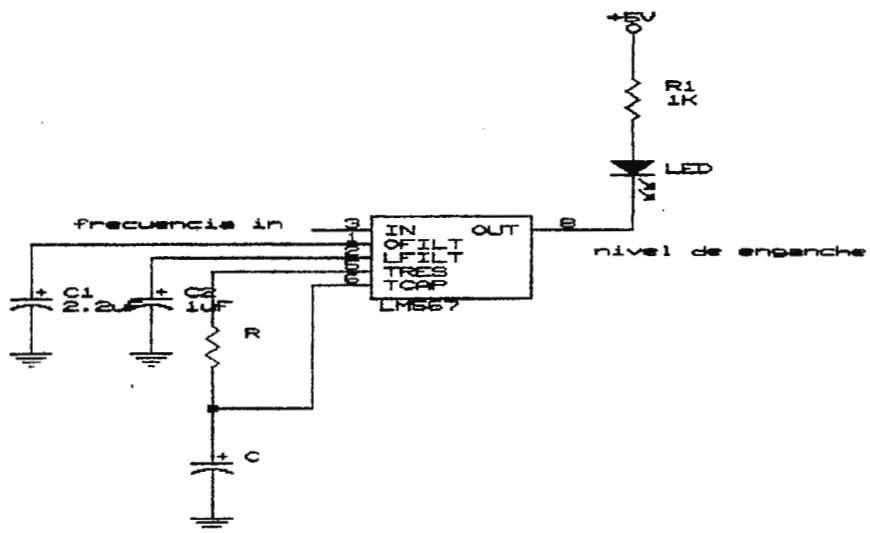


FIGURA 4

DETECTOR DE TONO

La salida de cada detector de tono pasa hacia un flip-flop tipo D que genera niveles TTL. Este dispositivo es el encargado de adecuar la respuesta del detector de tono en cuanto a interferencia de frecuencias y estabilidad en los cambios de órdenes (descenso y ascenso); posterior a este tratamiento, el pulso

proveniente del flip-flop se hace presente en los contadores ascendente/descendente (74LS193) en particular a las entradas UP/DOWN según se haya detectado o querido enviar la orden.

CONTADOR ASCENDENTE Y DESCENDENTE DE 8 BITS

Los contadores están conectados en cascada a modo de permitir el manejo de 8 bits para asegurar una resolución adecuada; el pulso inicial es recibido en la entrada ascendente del primer contador en cual es reflejado en la salida menos significativa del dispositivo y así sucesivamente hasta que se complete la cuenta máxima de 15 (2^4 –1) y se genere un bit de acarreo el cual pasa a la entrada ascendente del otro contador, que a su vez realizará su funcionamiento en la misma forma del anterior permitiendo así el manejo de una cuenta máxima de 255 (2^8 –1). De la misma manera pero en forma inversa un pulso en la entrada descendente del contador reduce la cuenta de uno en uno hasta cero, donde se genera un pulso de préstamo al siguiente contador. El pin de acarreo de primer contador esta conectado al pin de conteo ascendente del segundo. De la misma forma el pin de préstamo del primero se conecta al pin de conteo descendente del segundo.

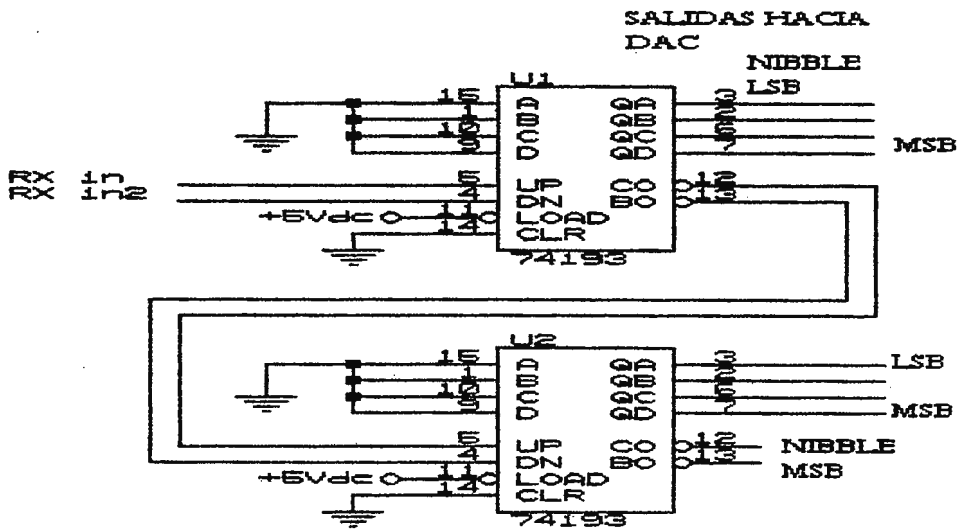


FIGURA 5

CONTADORES ASCENDENTES Y DESCENDENTES

CONVERTIDOR DE DIGITAL A ANALOGO

Este proceso da como resultado un byte el cual es introducido en el convertidor digital-análogo (DAC0806), dicha conversión brinda una corriente de salida proporcional a la entrada digital; esta corriente es convertida

en voltaje mediante el amplificador operacional (NTE858) en virtud de la tierra virtual que se genera en las entradas de éste. A8 es la entrada menos significativa y A1 la mas significativa.

Una vez obtenido este voltaje se define como la magnitud controlada y encargada de simular la salida del transductor y este mismo parámetro será realimentado hacia el punto de monitoreo.

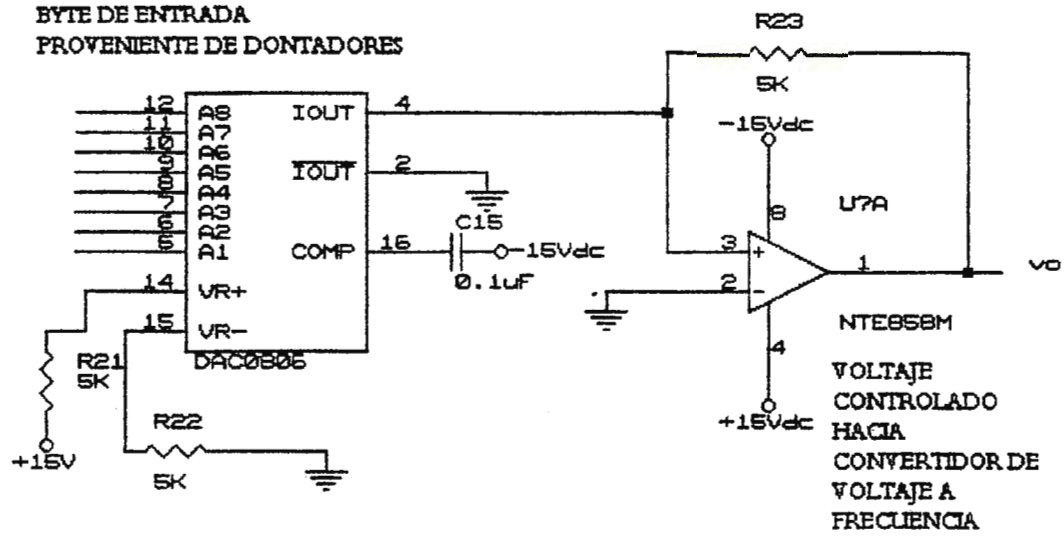


FIGURA 6

CONVERTIDOR DE DIGITAL A ANALOGO

Los voltajes de referencia del convertidor son 15V y tierra. Los pasos de voltaje se calcula con la siguiente fórmula:

$$Paso = \frac{(Vref(+) - Vref(-))}{(2^8 - 1)}$$

El voltaje de referencia positivo es 15V y el negativo tierra. Por lo tanto, los pasos de voltaje son de 0.05882 voltios.

TRANSMISOR DE FRECUENCIA

La forma de enviar este dato hacia el punto de visualización es a través de un convertidor de voltaje a frecuencia (LM331), siendo su salida máxima de 12 kHz a plena escala de entrada. El voltaje de entrada pin 7 es comparado con el voltaje del pin 6. Si el voltaje de entrada es superior al del pin 6 el comparador disparara un ONE SHOT TIMER. Una vez activo fluye una corriente por el pin 1 por un periodo t=1.1R6C3. Durante este tiempo fluye corriente del pin 1 al capacitor C4, esto eleva el voltaje en el pin 6 arriba del de entrada desconectando el timer. La magnitud de la corriente del pin 1 esta dada por

Vref/(POT1+R3). La salida de frecuencia (pin 3) esta conectada a la salida del timer colocándose en alto cuando se activa y bajo cuando se desactiva. La conexión de salida del pin tres esta conectada a la salida del timer por medio de un transistor internamente. La salida es un tren de pulsos con una amplitud de aproximadamente 0.25 voltios.

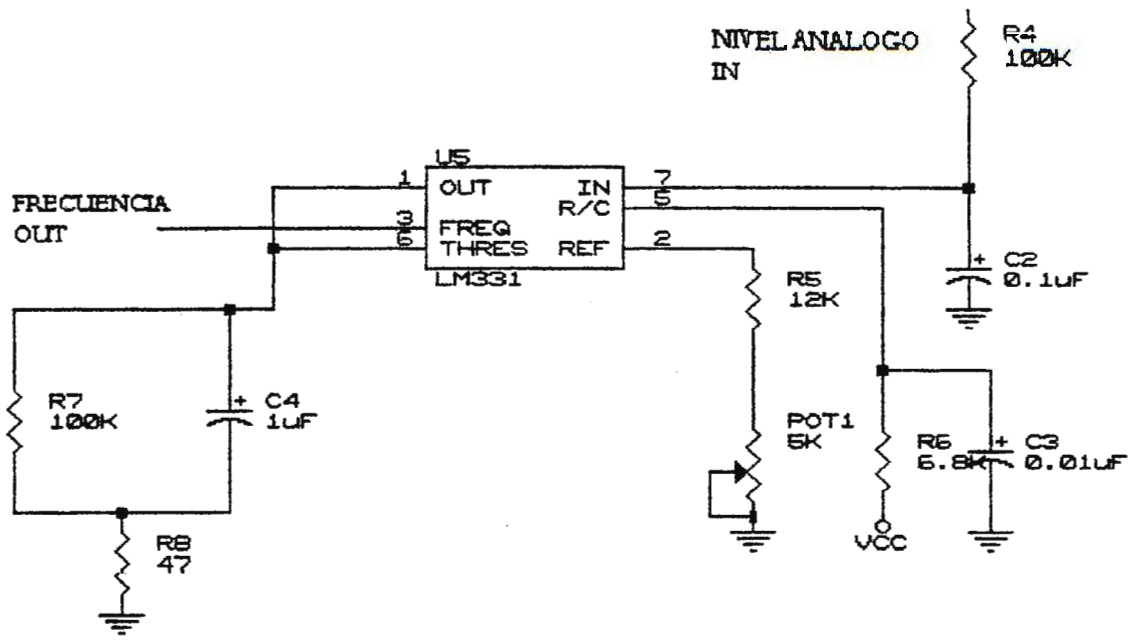


FIGURA 7

CONVERTIDOR DE VOLTAJE A FRECUENCIA

Posterior a esta conversión se diseño un comparador de voltaje (NTE858) para elevar la magnitud y definir más los pulsos cuadrados de salida, pues de no ser así se puede perder información en la etapa de recepción que sólo puede procesar señales de onda cuadrada en la fase de conversión de frecuencia a voltaje.

TRANSMISOR Y RECEPTOR

El transmisor mencionado como TX1 y TX2 son iguales, pero sintonizados a una frecuencia diferente. Lo mismo el par de receptores. Debido a su amplio rango de frecuencias se sintonizan fuera del rango comercial de FM (88 a 108 MHz).

TRANSMISOR

El transmisor es sintonizable en el rango de 80 a 110 MHz. Modula en FM con una ganancia y entapa de amplificación RF ajustables. La primera etapa del circuito constituido por los arreglos de Q1 y Q2 desarrollan un amplificador de audio de doble etapa y circuito de pre-énfasis. La otra etapa define la frecuencia de transmisión mezclándola y modulando la señal en FM. El transmisor utilizado es el siguiente:

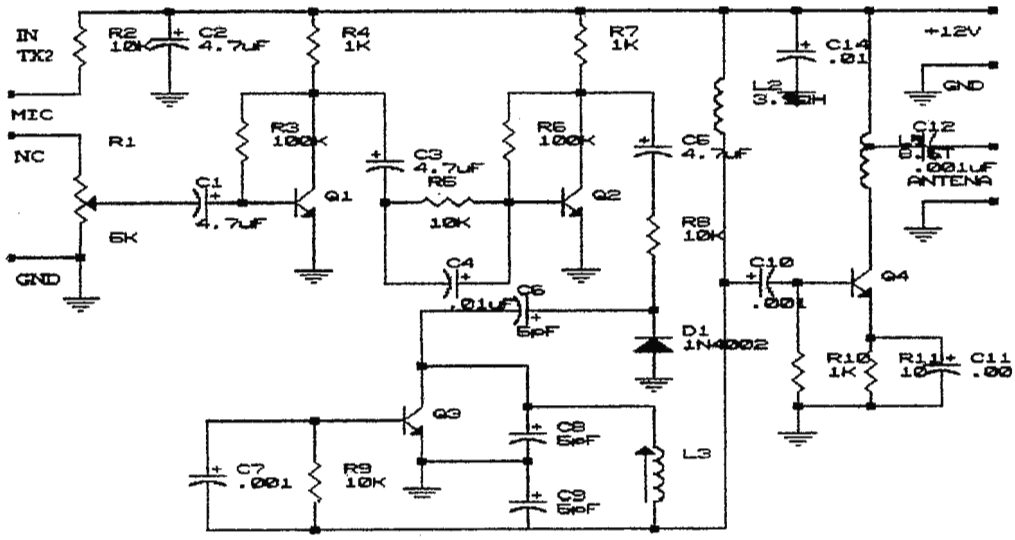


FIGURA 8

TRANSMISOR DE FM

RECEPTOR

El receptor es un receptor estándar de FM pero su rango de sintonía es de 70 hasta 110 MHz. Las señales capturadas por la antena son amplificadas por Q2, un transistor de alta ganancia y bajo ruido. Estas señales entran a NE-602 el cual convierte la señal a frecuencia intermedia de 10.7 MHz. Internamente en el NE-602 se encuentra un oscilador sintonizado por el circuito tanque: C11, C12, L1 y el varactor D1. El varactor actúa como un capacitor variable controlado por R12. La señal con frecuencia intermedia pasa por un filtro cerámico FL-1 para ser amplificada por Q1. Es demodulado por medio de detección de cuadratura por U1, C1 y L2 conforman el red de cambio de fase necesario para demodulación, obteniendo de esta manera la señal demodulada. A continuación esta el receptor de FM:

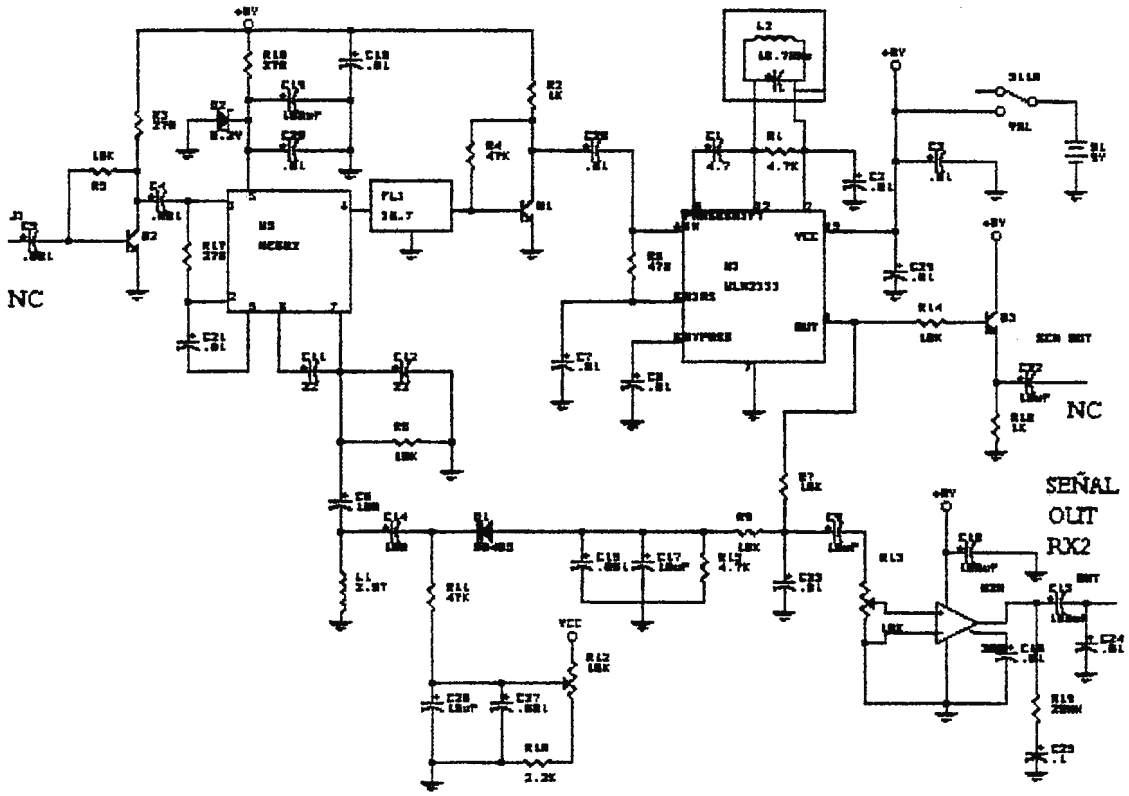


FIGURA 9

RECEPTOR DE FM

ALIMENTACION DEL CIRCUITO

El circuito necesita niveles de voltaje de 5, 15 y –15 voltios. Según el lugar y localización del dispositivo se presentan dos alternativas de alimentación. La primera utiliza baterías de 9V, necesitando 4 para cumplir con los niveles de voltaje y demanda de potencia. Los LM7815, LM7805 y LM7915 utilizados proporcionan un nivel de voltaje de salida estable a pesar de variaciones en sus entradas. El 7815 regula el nivel de voltaje a su entrada a 15 VDC, el 7805 a 5 VDC y el 7915 cuyo voltaje de entrada debe ser negativo regula a –15 VDC. Cada regulador de voltaje tiene a su salida un filtro para reducir el rizado. Esta opción tiene como ventaja la fácil movilización del dispositivo siendo independiente y más versátil. Pero el costo de utilización se eleva por el uso continuo de las baterías. A continuación se presenta el arreglo utilizado para esta opción:

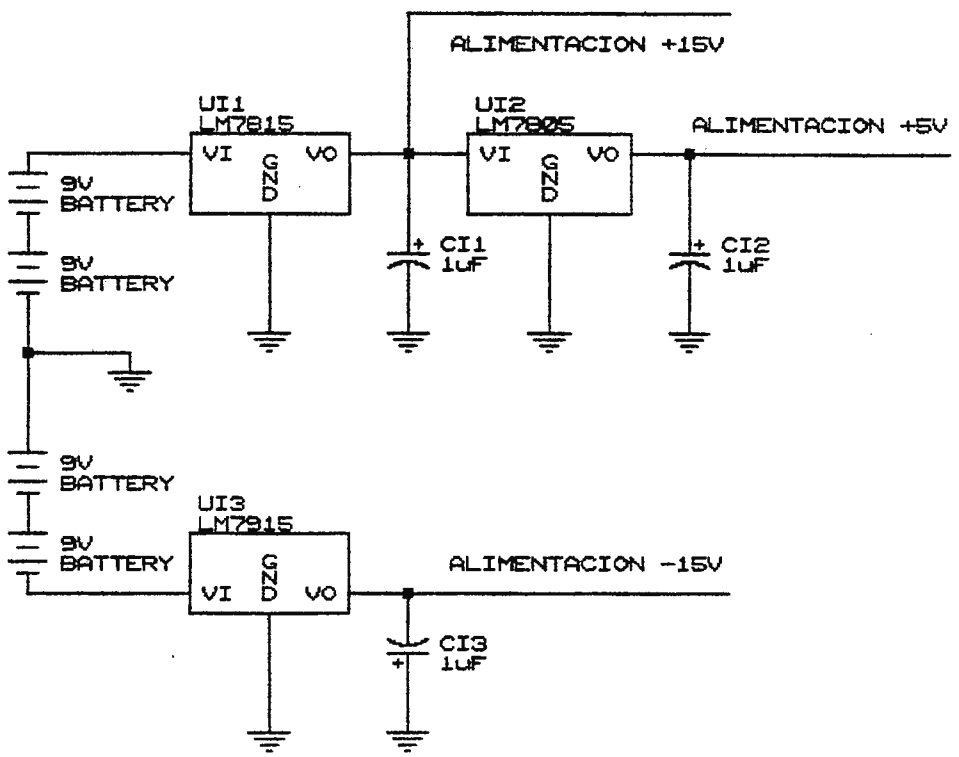


FIGURA 10
ALIMENTACION CON BATERIAS

La segunda opción utiliza la red de alimentación de 110 VAC, la cual es procesada (rectificada, filtrada y regulada). La señal es atenuada por un transformador con toma central, a un nivel de aproximádamente 36 VAC y proporciona la capacidad de obtener los niveles positivos y negativos necesarios de una misma fuente alterna; ambos extremos de la toma son rectificados por un puente de diodos para obtener un nivel de voltaje continuo, para reducir rizado a la salida de cada puente se coloca un filtro y de esa forma se

proporciona un nivel de voltaje directo negativo y positivo para ser acondicionado por los reguladores de voltaje.

El diagrama es el siguiente:

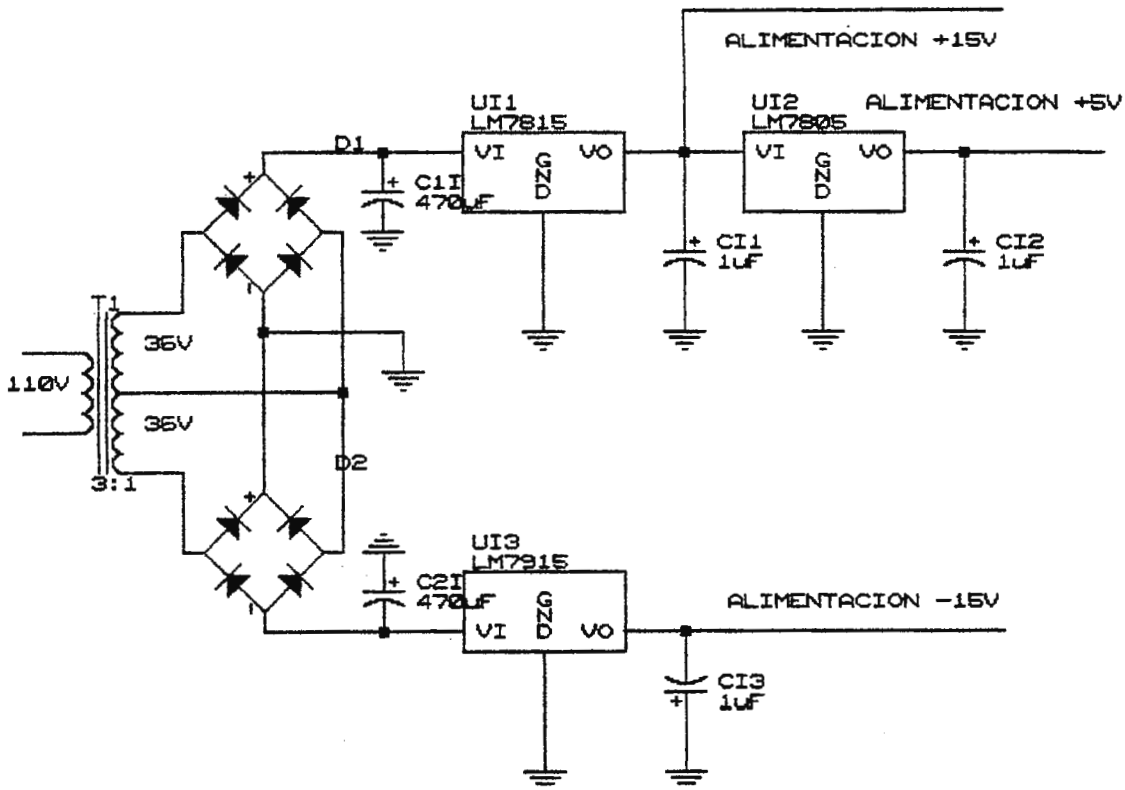


FIGURA 11

ALIMENTACION CON RED ALTERNA DE 110Vrms

ESQUEMA DE CIRCUITOS IMPRESOS

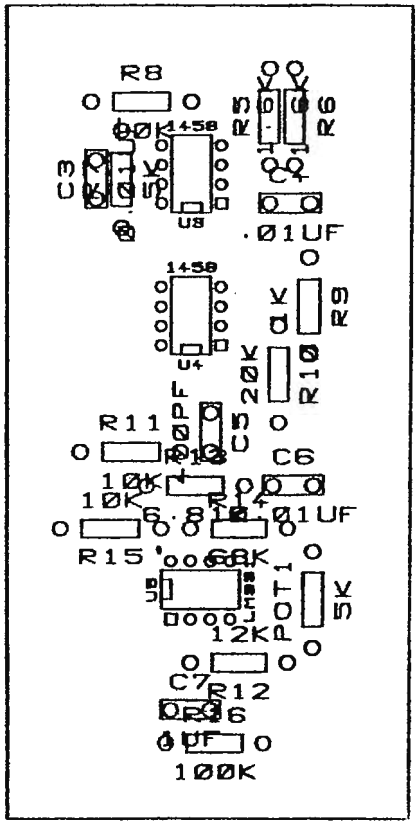
La elaboración de los circuitos impresos se hizo con la ayuda de software y el esquema de los circuitos se elaboró utilizando ORCAD y para generar el diseño de las pistas se exportó el diagrama al programa PCB. Al exportar el esquema de ORCAD a PCB se obtuvo el listado completo de componentes a utilizar para insertar en la pantalla y con el listado de componentes se seleccionó la dimensión correspondiente a cada elemento en el circuito impreso. Esto facilita las cosas ya que se obtiene un conjunto de todos los componentes del circuito con sus respectivos valores para ordenar. Con los componentes ordenados en la pantalla se procede a desarrollar las pistas que los conectan para ambos lados de la tarjeta y una vez desarrollado el esquema completo se revisa las pistas para que exista una distancia adecuada entre ellas, debido a que aparentemente las pistas son correctas pero están demasiado cerca de otras pistas o componentes, reduciendo de esta manera contactos no deseados en la tarjeta. Al concluir el proceso de depuración de errores se fabrican las tarjetas.

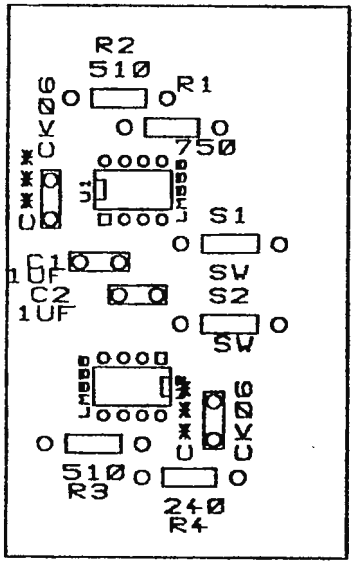
Cada cara individualmente es quemada en la tarjeta y el cobre excedente es retirado con ácido. La tarjeta es limpiada, pulida y revisada para taladrar.

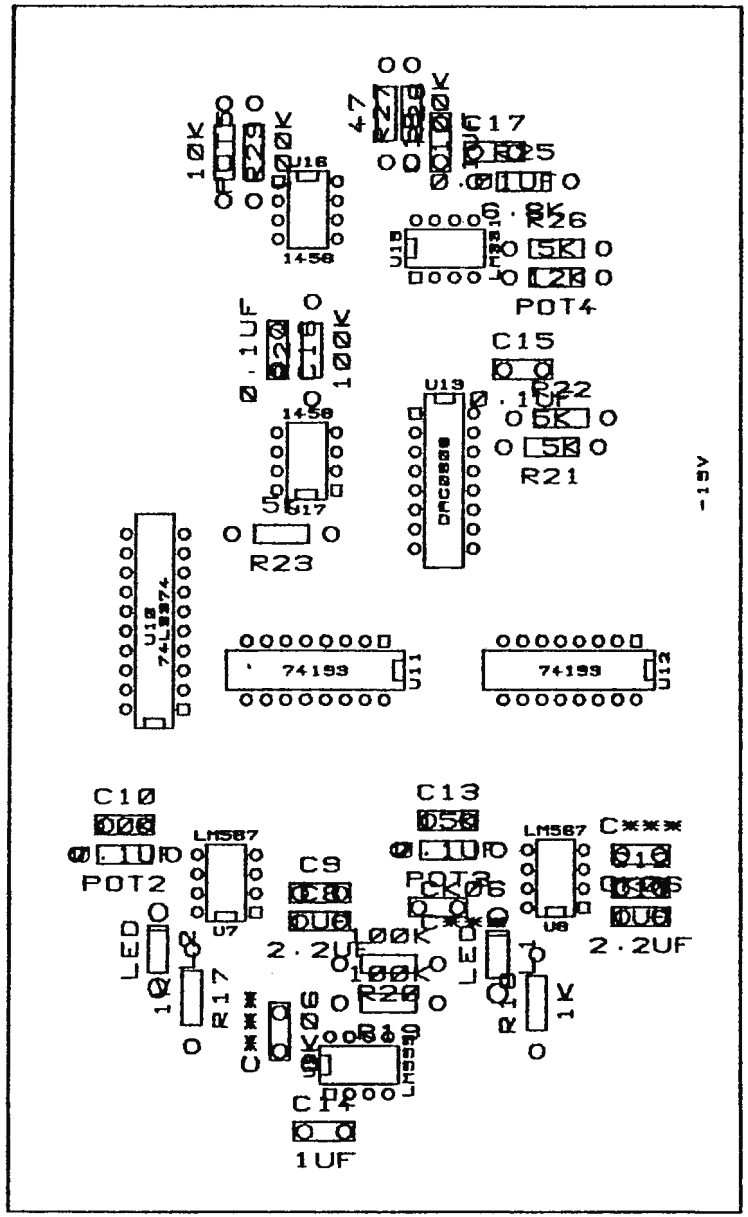
En las siguientes tres páginas se presenta el esquema del circuito impreso desarrollado en tres partes:

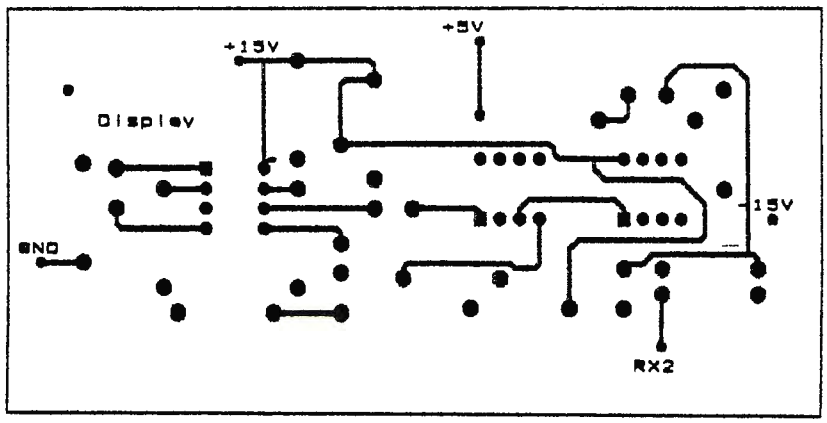
La primera página contiene el conjunto de componentes utilizados según su localización en la tarjeta y con sus respectivos valores.

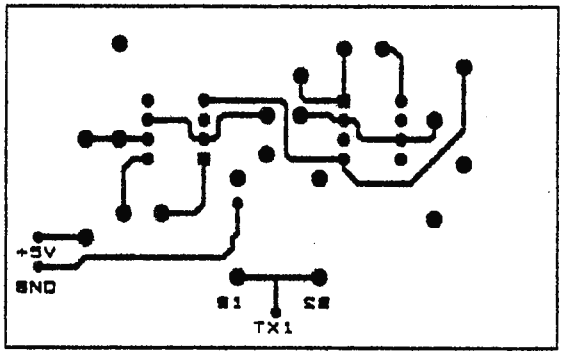
Las siguientes dos páginas presentan el esquema de las pistas de cada cara del circuito.

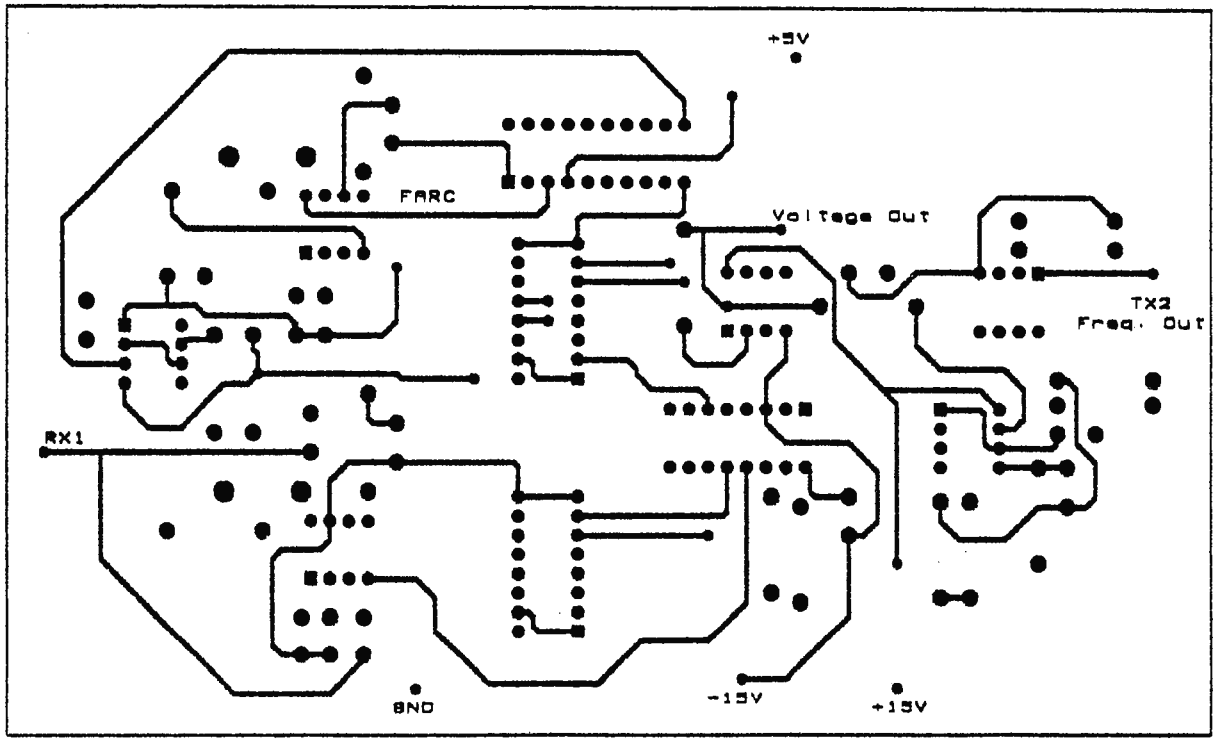

R8
R5
R6
C3
.01UF
R9
R10
C5
R11
C6
R14
R15
POT1
12K
C7
R12
100K

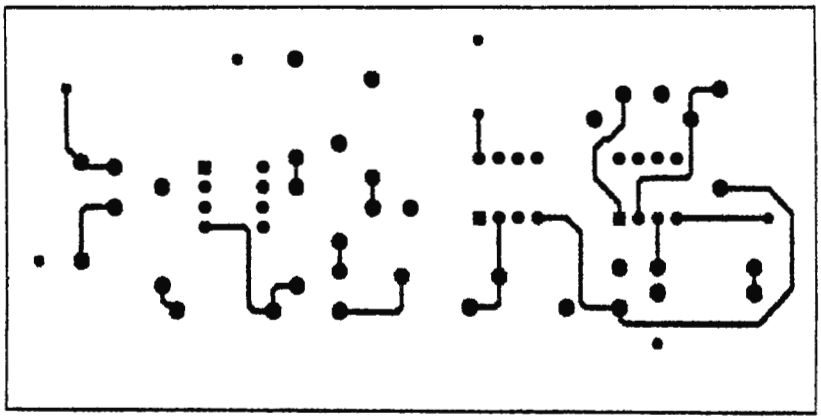

R2
510
R1
750
S1
SW
S2
SW
C1
1UF
C2
1UF
R3
510
R4
240

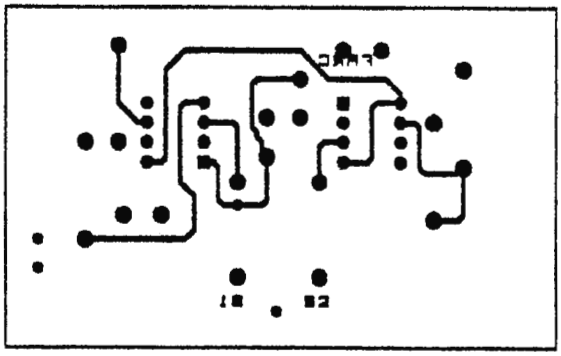

10K
R23
R27
47
C17
.01UF
R26
5K
POT4
C15
.1UF
C22
R21
-15V
74193
74193
C10
POT2
C13
POT3
C9
2.2UF
2.2UF
LED
LED
R17
R20
C14
1UF

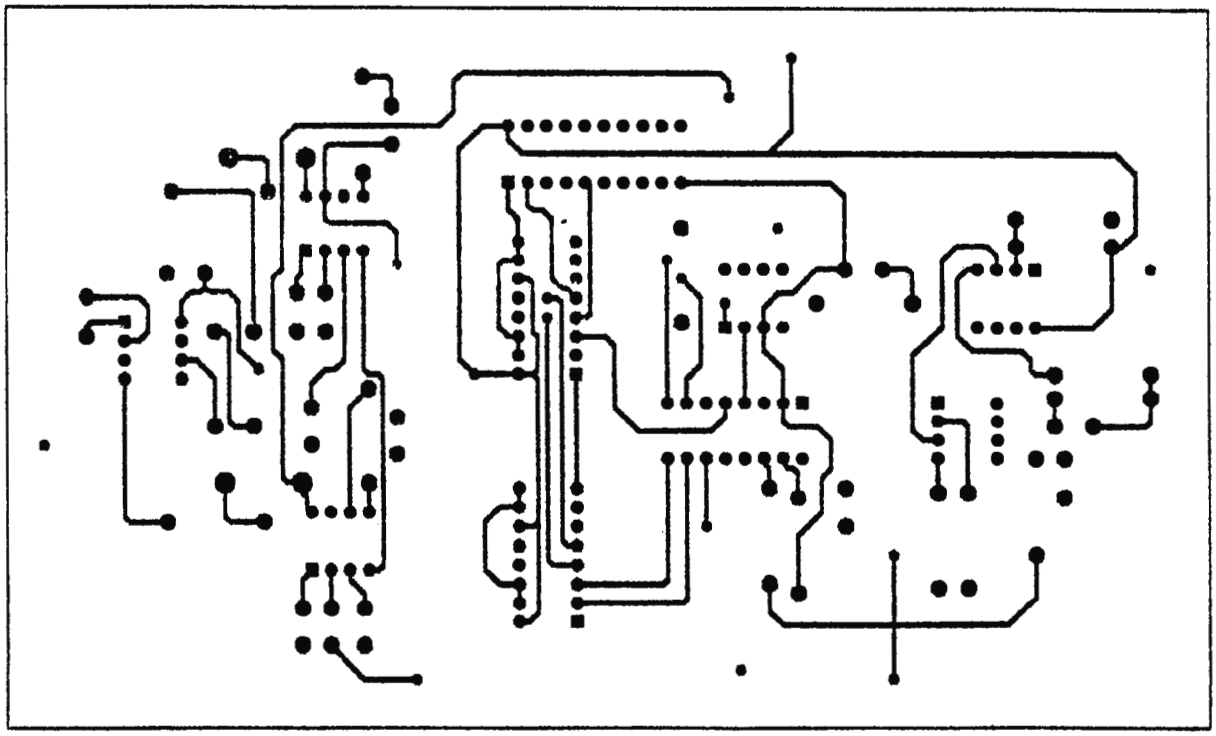

+5V
+15V
Display
GND
-15V
RX2


+5V
GND
S1
S2
TX1


+5V
FARC
Voltage Out
TX2
Freq. Out
RX1
GND
-15V
+15V







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National Semiconductor

May 1997

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

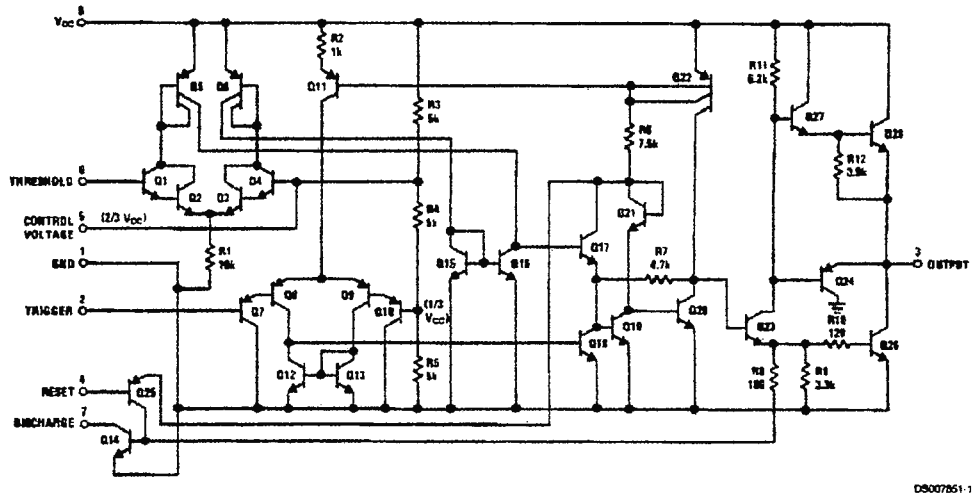
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8 pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555H, LM555CH	760 mW
LM555, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to + 125°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞		10	12		10	15	mA
	(Low State) (Note 4)							
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ,		30			50		ppm/°C
	C = 0.1 µF, (Note 5)							
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ,		90			150		ppm/°C
	C = 0.1 µF, (Note 5)							
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	µA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 7)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°C/W (T0-5), 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

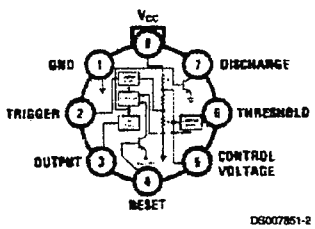
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

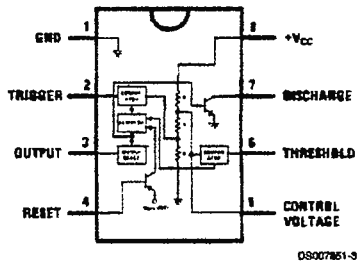
Metal Can Package



DS007851-2

Top View
Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages

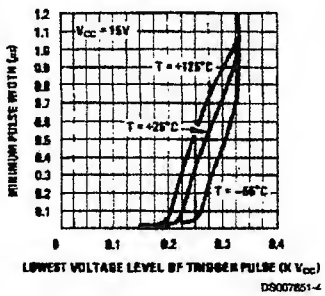


DS007851-3

Top View
Order Number LM555J, LM555CJ, LM555CM, LM555CMM or LM555CN
See NS Package Number J08A, M08A, MUA08A or N08E

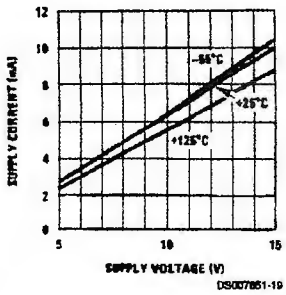
Typical Performance Characteristics

Minimum Pulse Width Required for Triggering



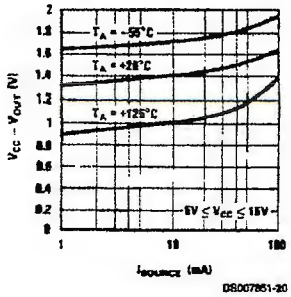
DS007851-4

Supply Current vs Supply Voltage



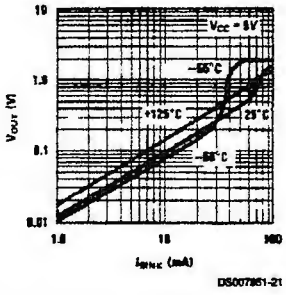
DS007851-19

High Output Voltage vs Output Source Current



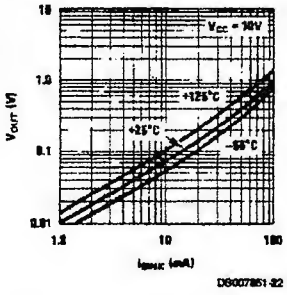
DS007851-20

Low Output Voltage vs Output Sink Current



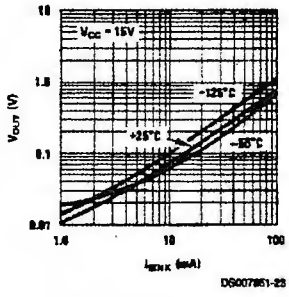
DS007851-21

Low Output Voltage vs Output Sink Current



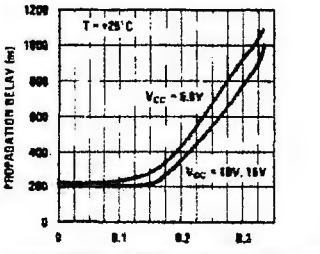
DS007851-22

Low Output Voltage vs Output Sink Current



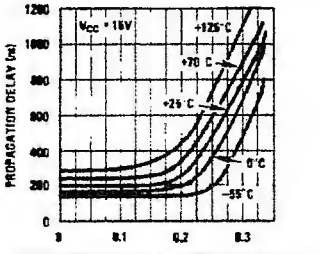
DS007851-23

Output Propagation Delay vs Voltage Level of Trigger Pulse



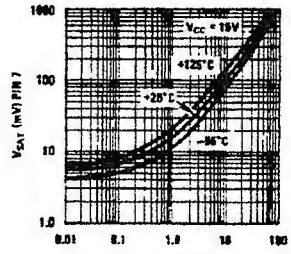
DS007851-24

Output Propagation Delay vs Voltage Level of Trigger Pulse



DS007851-25

Discharge Transistor (Pin 7) Voltage vs Sink Current



DS007851-26

National Semiconductor

February 1995

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

Metal Can Package

TL/H/6975–1

Top View

Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages

TL/H/6975–2

Top View

Order Number LM567CM
See NS Package Number M08A

Order Number LM567CN
See NS Package Number N08E

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 1)	1100 mW
V_8	15V
V_3	−10V
V_3	V_4 + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM567H	−55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics AC Test Circuit, T_A = 25°C, V^+ = 5V

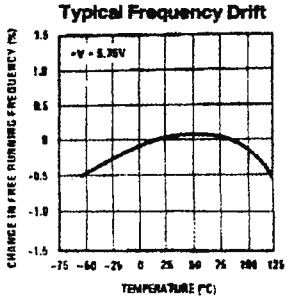
Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	i_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	i_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 − 6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75–5.75V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ±60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V − 6.75V 4.75V − 9V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

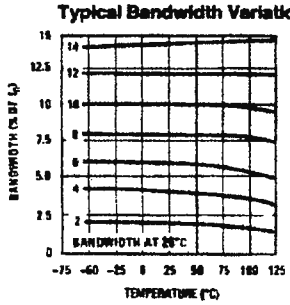
Note 2: Refer to RETS567X drawing for specifications of military LM567H version.

Typical Performance Characteristics

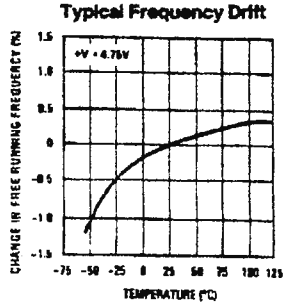
Typical Frequency Drift



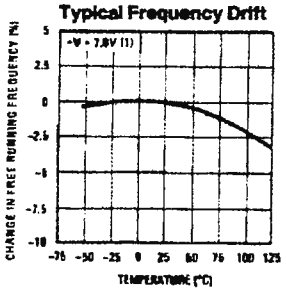
Typical Bandwidth Variation



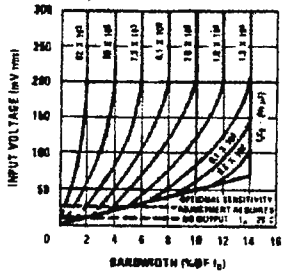
Typical Frequency Drift



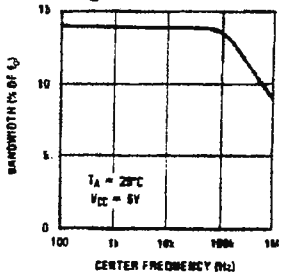
Typical Frequency Drift



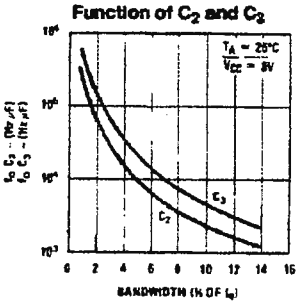
Bandwidth vs Input Signal Amplitude



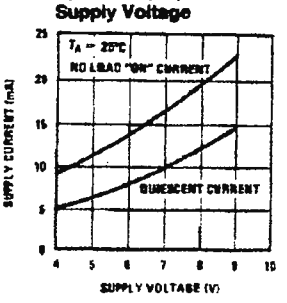
Largest Detection Bandwidth



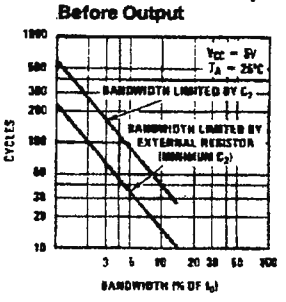
Detection Bandwidth as a Function of C_2 and C_3



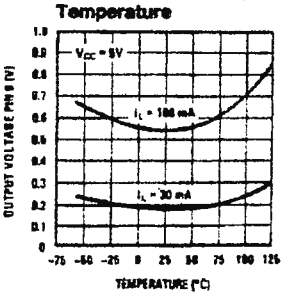
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output



Typical Output Voltage vs Temperature



TL/H/6975–4

National Semiconductor

December 1994

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

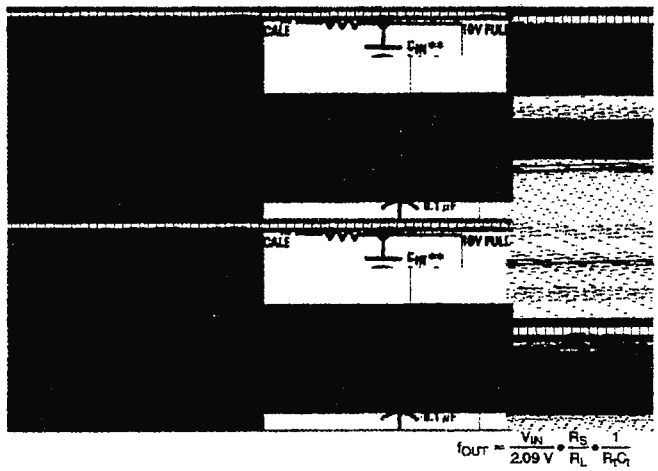
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



$$f_{OUT} = \frac{V_{IN}}{2.09\,V} \cdot \frac{R_S}{R_L} \cdot \frac{1}{R_T C_T}$$

TL/H/5680–1

*Use stable components with low temperature coefficients. See Typical Applications section.

**0.1 μF or 1 μF, See "Principles of Operation."

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	−0.2V to +V_S	−0.2V to +V_S	−0.2V to +V_S
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW		
θ_{JA}	150°C/W		
(N Package) P_D		1.25W	1.25W
θ_{JA}		100°C/W	100°C/W
(M Package) P_D		1.25W	
θ_{JA}		85°C/W	
Lead Temperature (Soldering, 10 sec.)			
Dual-In-Line Package (Plastic)	260°C	260°C	260°C
Metal Can Package (TO-5)	260°C		
ESD Susceptibility (Note 4)			
Metal Can Package (TO-5)	2000V		
Other Packages		500V	500V

Electrical Characteristics T_A = 25°C unless otherwise specified (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
VFC Non-Linearity (Note 3)	4.5V ≤ V_S ≤ 20V		±0.003	±0.01	% Full-Scale
	T_{MIN} ≤ T_A ≤ T_{MAX}		±0.006	±0.02	% Full-Scale
VFC Non-Linearity In Circuit of *Figure 1*	V_S = 15V, f = 10 Hz to 11 kHz		±0.024	±0.14	%Full-Scale
Conversion Accuracy Scale Factor (Gain)	V_{IN} = −10V, R_S = 14 kΩ				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	T_{MIN} ≤ T_A ≤ T_{MAX}, 4.5V ≤ V_S ≤ 20V				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	4.5V≤V_S ≤ 10V		0.01	0.1	%/V
	10V ≤ V_S ≤ 40V		0.006	0.06	%/V
Rated Full-Scale Frequency	V_{IN} = −10V	10.0			kHz
Gain Stability vs Time (1000 Hrs)	T_{MIN} ≤ T_A ≤ T_{MAX}		±0.02		% Full-Scale
Overrange (Beyond Full-Scale) Frequency	V_{IN} = −11V	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	T_{MIN} ≤ T_A ≤ T_{MAX}		±4	±14	mV
LM131A/LM231A/LM331A	T_{MIN} ≤ T_A ≤ T_{MAX}		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	T_{MIN} ≤ T_A ≤ T_{MAX}	−0.2		V_{CC}−2.0	V

Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2) (Continued)

Parameter	Conditions	Min	Typ	Max	Units
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	$\times V_S$
Input Bias Current, Pin 5	V_S = 15V				
All Devices	$0V \le V_{PIN\,5} \le 9.9V$		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\,5}$ = 10V		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\,5}$ = 10V		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\,1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	µA
LM331, LM331A		116	136	156	µA
Change with Voltage	$0V \le V_{PIN\,1} \le 10V$		0.2	1.0	µA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		µA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	I = 5 mA		0.15	0.50	V
	$I = 3.2\ mA$ (2 TTL Loads), $T_{MIN} \le T_A \le T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	µA
SUPPLY CURRENT					
LM131, LM131A, LM231,	V_S = 5V	2.0	3.0	4.0	mA
LM231A	V_S = 40V	2.5	4.0	6.0	mA
LM331, LM331A	V_S = 5V	1.5	3.0	6.0	mA
	V_S = 40V	2.0	4.0	8.0	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All specifications apply in the circuit of *Figure 3*, with $4.0V \le V_S \le 40V$, unless otherwise noted.

Note 3: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times$ (10 kHz/−10 V_{DC}) when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon®, or polystyrene.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

National Semiconductor

April 1998

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

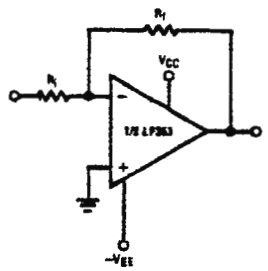
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 10 mV
- Low input bias current: 50pA
- Low input noise voltage: 25 nV/$\sqrt{Hz}$
- Low input noise current: 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 3.6 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion A_V=10,: <0.02% RL=10k, V_O=20Vp-p, BW=20 Hz-20 kHz
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

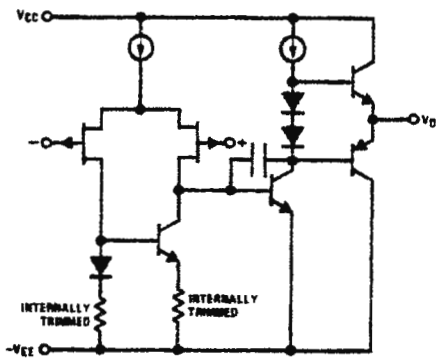
Typical Connection



DS005649-14

Simplified Schematic

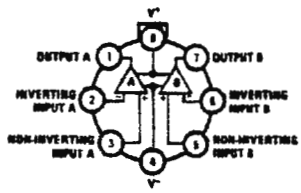
1/2 Dual



DS005649-16

Connection Diagrams

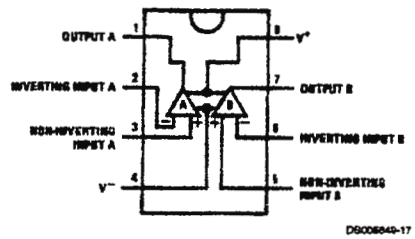
Metal Can Package



DS005649-15

Top View
Order Number LF353H
See NS Package Number H08A

Dual-In-Line Package



DS005649-17

Top View
Order Number LF353M or LF353N
See NS Package Number M08A or N08E

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1700V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 5, 6)		25	100	pA
		T_j≤70°C			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 5, 6)		50	200	pA
		T_j≤70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω,		16		nV/$\sqrt{\text{Hz}}$
		f=1000 Hz				
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/$\sqrt{\text{Hz}}$

Note 2: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the N package, and 158°C/W typ junction to ambient for the H package.

AC Electrical Characteristics (Continued)

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for V_S=±15V and 0°C≤T_A≤+70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM}=0.

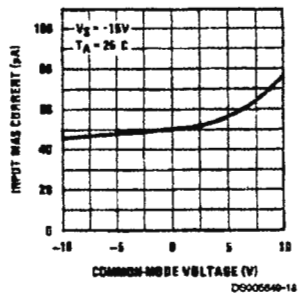
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

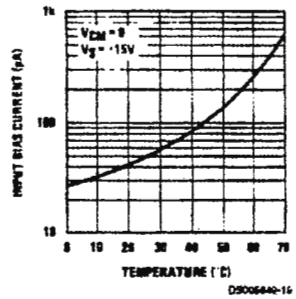
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

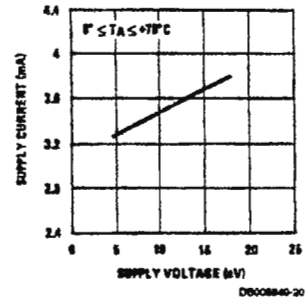
Input Bias Current



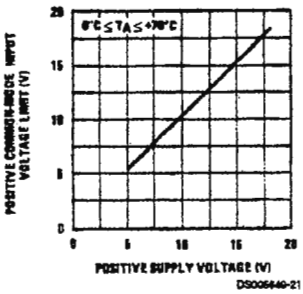
Input Bias Current



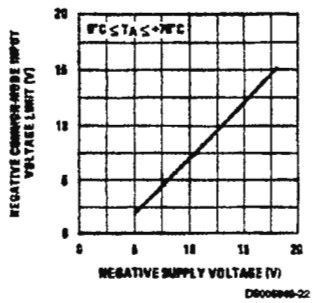
Supply Current



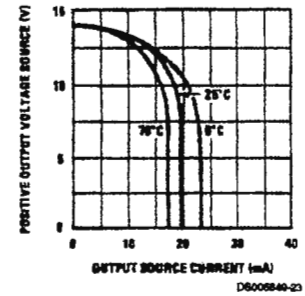
Positive Common-Mode Input Voltage Limit



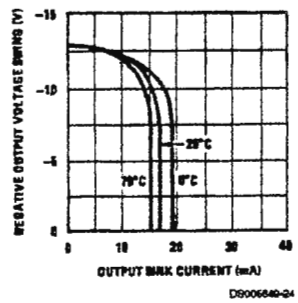
Negative Common-Mode Input Voltage Limit



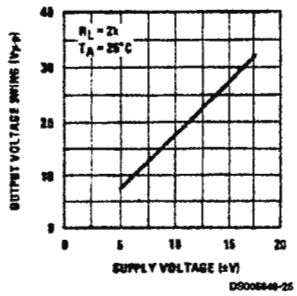
Positive Current Limit



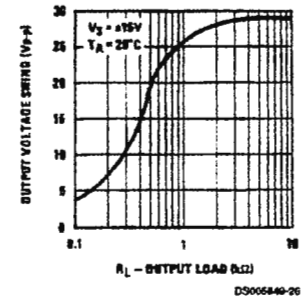
Negative Current Limit



Voltage Swing

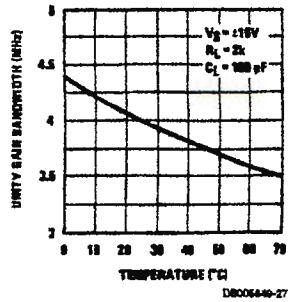


Output Voltage Swing



Typical Performance Characteristics (Continued)

Gain Bandwidth



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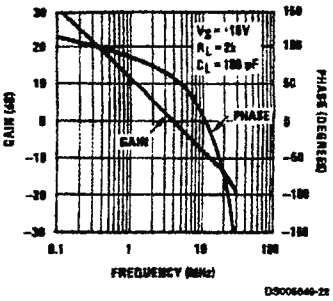
Bode Plot



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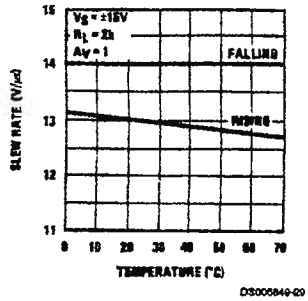
Slew Rate



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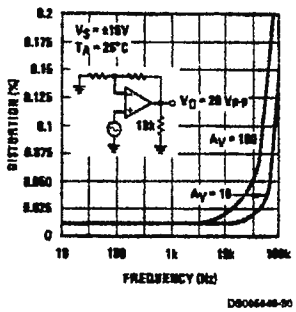
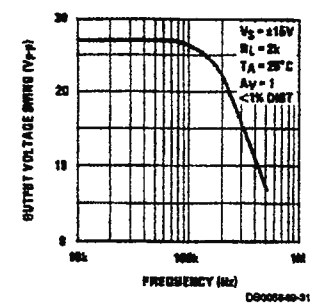
Distortion vs Frequency



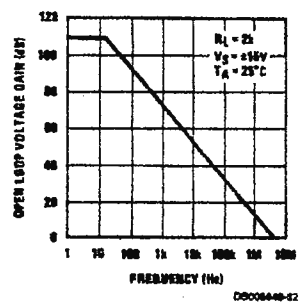
DS005640-30

Undistorted Output-Voltage Swing



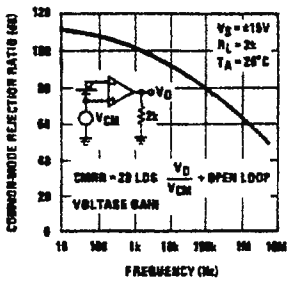
DS005640-31

Open Loop Frequency Response



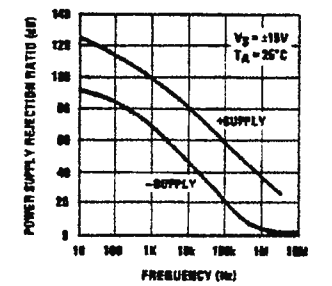
DS005640-32

Common-Mode Rejection Ratio



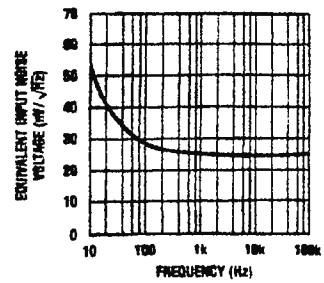
DS005640-33

Power Supply Rejection Ratio



DS005640-34

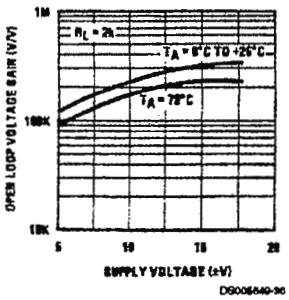
Equivalent Input Noise Voltage



DS005640-35

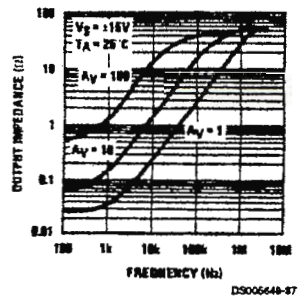
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain (V/V)



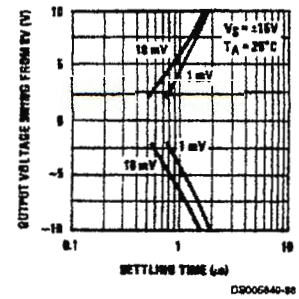
DS005640-36

Output Impedance



DS005640-37

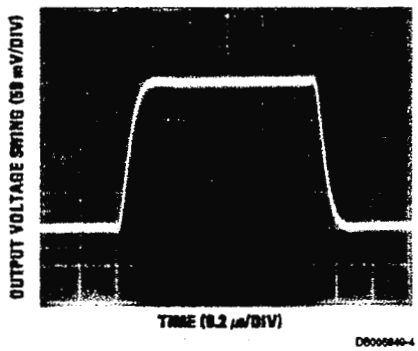
Inverter Settling Time



DS005640-38

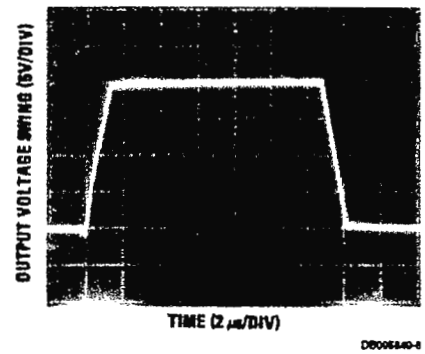
Pulse Response

Small Signaling Inverting



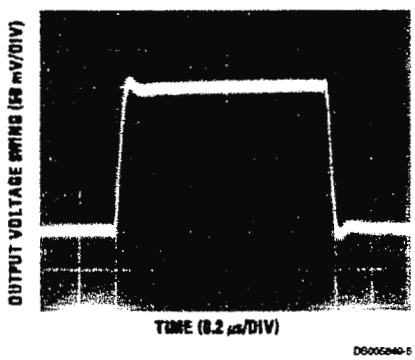
DS005640-4

Large Signal Inverting



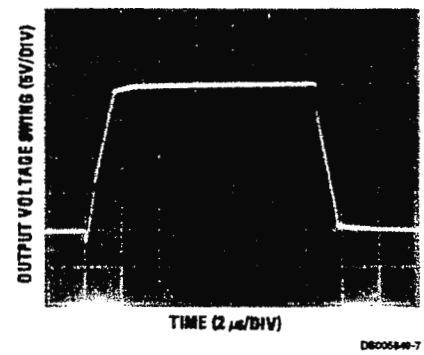
DS005640-6

Small Signal Non-Inverting



DS005640-5

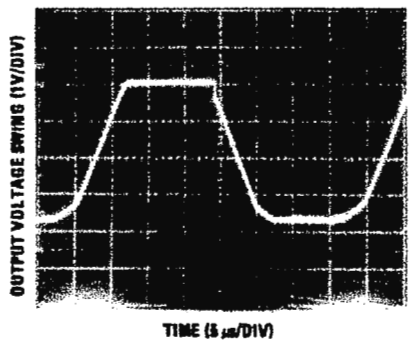
Large Signal Non-Inverting



DS005640-7

Pulse Response (Continued)

Current Limit (R_L = 100Ω)



D5006440-6

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

National Semiconductor

January 1995

DAC0808/DAC0807/DAC0806 8-Bit D/A Converters

General Description

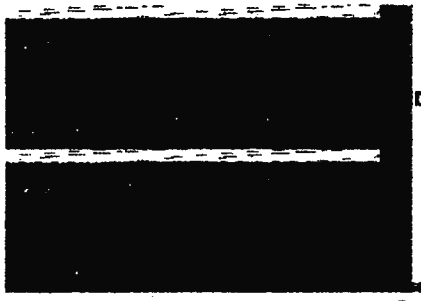
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/ 256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

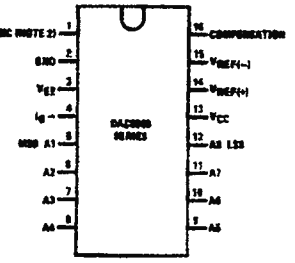
Block and Connection Diagrams



5687–1

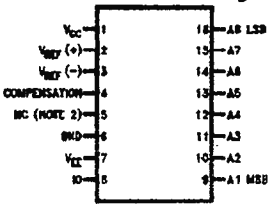
Order Number DAC0808, DAC0807, or DAC0806
See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/H/5687–2

Small-Outline Package



TL/H/5687–13

Top View

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS				
		J PACKAGE (J16A)*		N PACKAGE (N16A)*		SO PACKAGE (M16A)
				DAC0808LCN	MC1408P8	DAC0808LCM
7-bit	$0°C \leq T_A \leq +75°C$	DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7	DAC0807LCM
6-bit	$0°C \leq T_A \leq +75°C$	DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6	DAC0806LCM

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 3)	1000 mW
ESD Susceptibility (Note 4)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808LC Series	$0 \le T_A \le +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808LC (LM1408-8)				**±0.19**	%
	DAC0807LC (LM1408-7), (Note 5)				±0.39	%
	DAC0806LC (LM1408-6), (Note 5)				±0.78	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A = 25°C (Note 6), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω,				
		(Figure 3)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance (Note 2)	$E_r \le 0.19\%$, T_A = 25°C				
	V_{EE} = −5V, I_{REF} = 1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

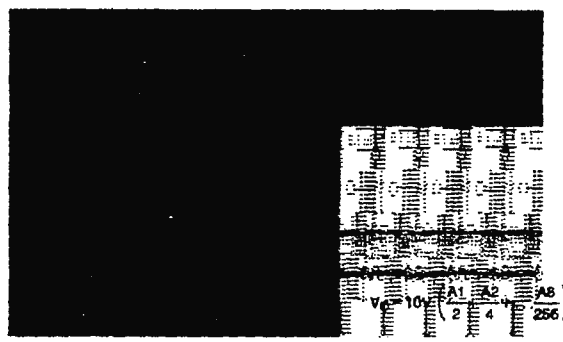
Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: All current switches are tested to guarantee at least 50% of rated current.

Note 6: All bits switched.

Note 7: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application



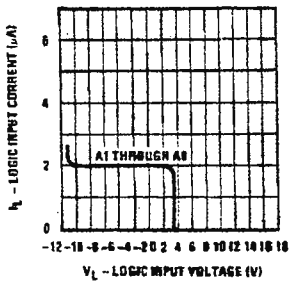
TL/H/5687–9

FIGURE 1. +10V Output Digital to Analog Converter (Note 7)

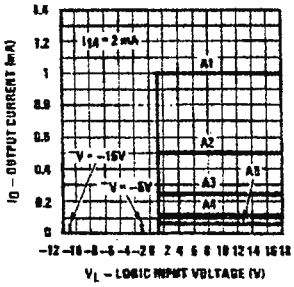
Typical Performance Characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

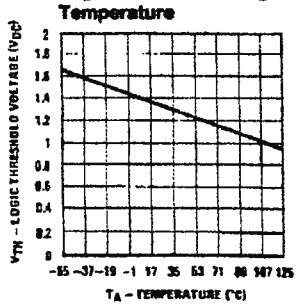
Logic Input Current vs Input Voltage



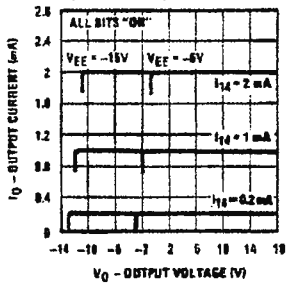
Bit Transfer Characteristics



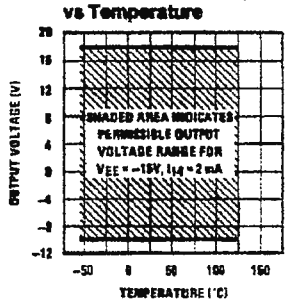
Logic Threshold Voltage vs Temperature



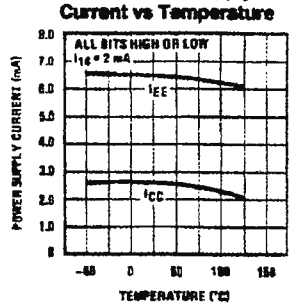
Output Current vs Output Voltage (Output Voltage Compliance)



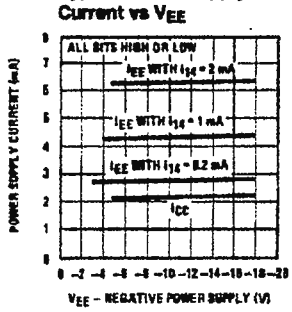
Output Voltage Compliance vs Temperature



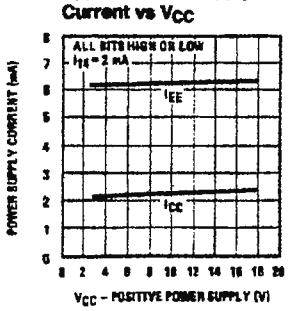
Typical Power Supply Current vs Temperature



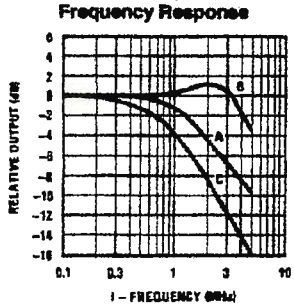
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



TL/H/5687–5

Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

National Semiconductor

February 1988

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BM and CD40192BC are BCD counters, while the CD40193BM and CD40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

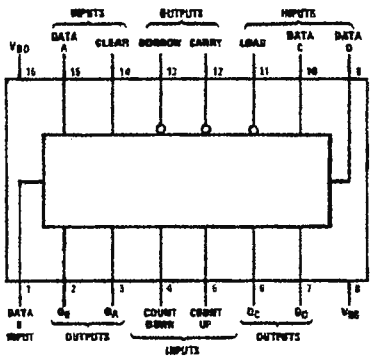
All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Carry and borrow outputs for easy expansion to N-bit by cascading
- Asynchronous clear
- Equivalent to — MM54C192/MM74C192 and MM54C193/MM74C193

Connection Diagram

Dual-In-Line Package

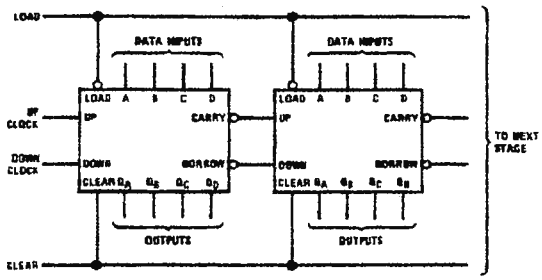


TL/F/5988–1

Top View

Order Number CD40192B or CD40193

Cascading Packages



TL/F/5988–2

 TL/F/5988

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD}+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-in-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40192BM, CD40193BM	$-55°C$ to $+125°C$
CD40192BC, CD40193BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD40192BM/CD40193BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		5			5		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		10			10		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$		0.05			0.05		0.05	V
		$V_{DD}=10V$		0.05			0.05		0.05	V
		$V_{DD}=15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$	4.95		4.95			4.95		V
		$V_{DD}=10V$	9.95		9.95			9.95		V
		$V_{DD}=15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD}=10V, V_O=1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD}=10V, V_O=1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V, V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V, V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V, V_O=9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD}=15V, V_O=13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V, V_{IN}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V, V_{IN}=15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD40192BC/CD40193BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		20			20		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		40			40		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$		0.05			0.05		0.05	V
		$V_{DD}=10V$		0.05			0.05		0.05	V
		$V_{DD}=15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$	4.95		4.95			4.95		V
		$V_{DD}=10V$	9.95		9.95			9.95		V
		$V_{DD}=15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD}=10V, V_O=1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD}=10V, V_O=1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V, V_O=1.5V$	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics CD40192BC/CD40193BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, input t_r = t_f = 20 ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Count Up or Count Down to Q	V_{DD} = 5V		250	400	ns
		V_{DD} = 10V		100	160	ns
		V_{DD} = 15V		80	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Count Up to Carry	V_{DD} = 5V		120	200	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	65	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Count Down to Borrow	V_{DD} = 5V		120	200	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	65	ns
t_{SU}	Time Prior to Load That Data Must Be Present	V_{DD} = 5V		100	160	ns
		V_{DD} = 10V		30	50	ns
		V_{DD} = 15V		25	40	ns
t_{PHL}	Propagation Delay Time from Clear to Q	V_{DD} = 5V		130	220	ns
		V_{DD} = 10V		60	100	ns
		V_{DD} = 15V		50	80	ns
t_{PLH} or t_{PHL}	Propagation Delay Time from Load to Q	V_{DD} = 5V		300	480	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		95	150	ns
t_{TLH} or t_{THL}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Count Frequency	V_{DD} = 5V	2.5	4		MHz
		V_{DD} = 10V	6	10		MHz
		V_{DD} = 15V	7.5	12.5		MHz
t_{rCL} or t_{fCL}	Maximum Count Rise or Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	5			μs
		V_{DD} = 15V	1			μs
t_{WH}, t_{WL}	Minimum Count Pulse Width	V_{DD} = 5V		120	200	ns
		V_{DD} = 10V		35	80	ns
		V_{DD} = 15V		28	65	ns
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		300	480	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		95	150	ns
t_{WL}	Minimum Load Pulse Width	V_{DD} = 5V		100	160	ns
		V_{DD} = 10V		40	65	ns
		V_{DD} = 15V		32	55	ns
C_{IN}	Average Input Capacitance	Load and Data Inputs (A,B,C,D)		5	7.5	pF
		Count Up, Count Down and Clear		10	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

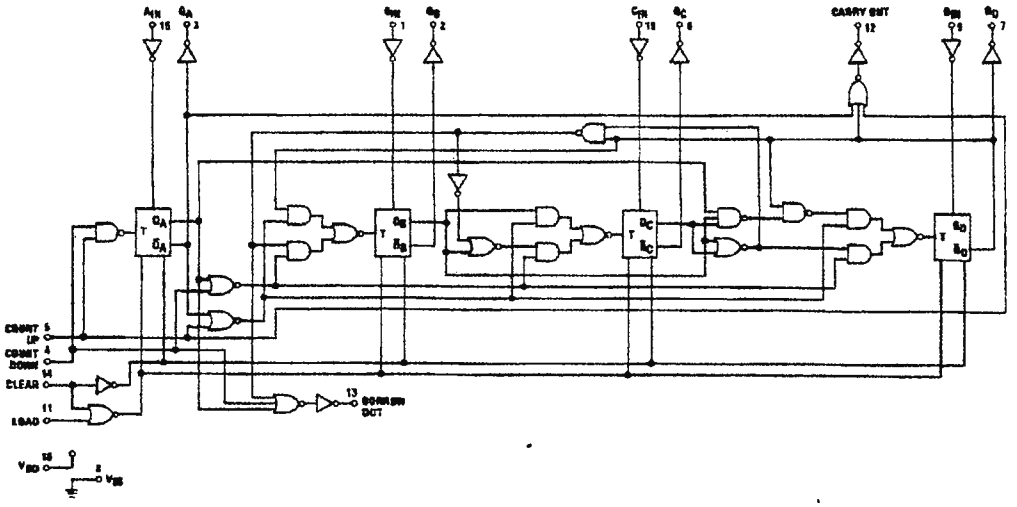
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Schematic Diagrams

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter



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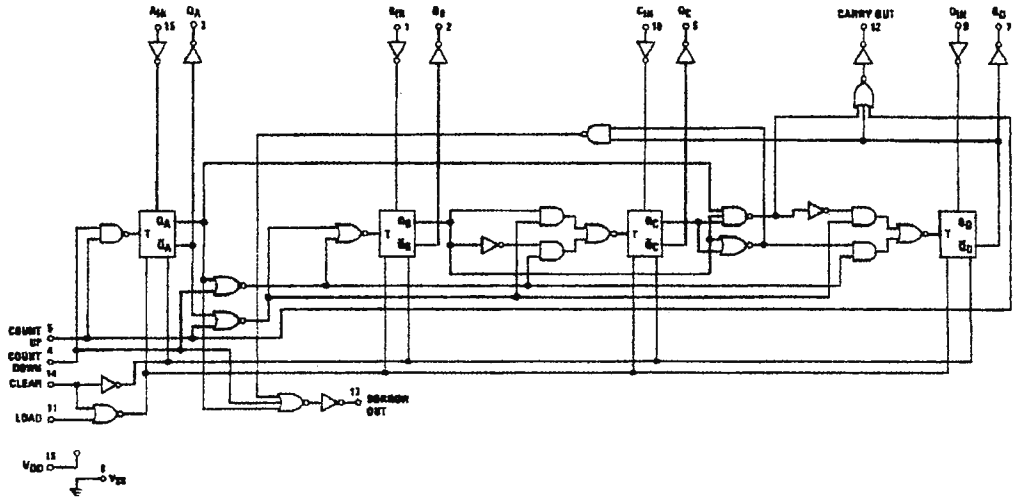
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter



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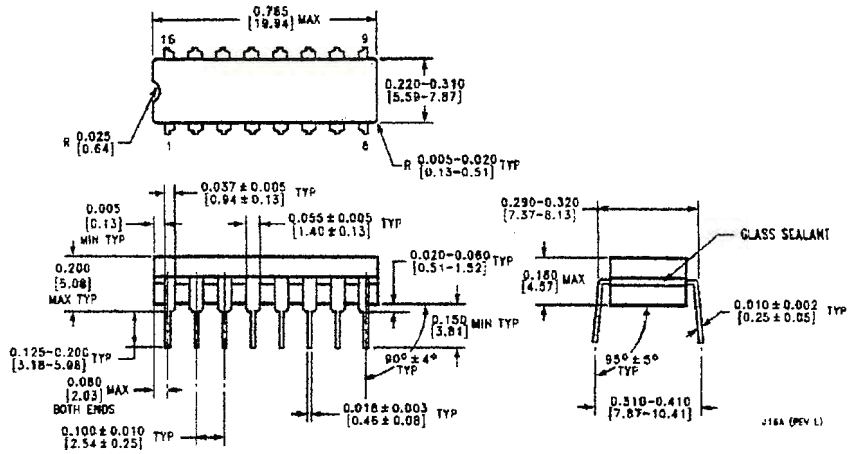
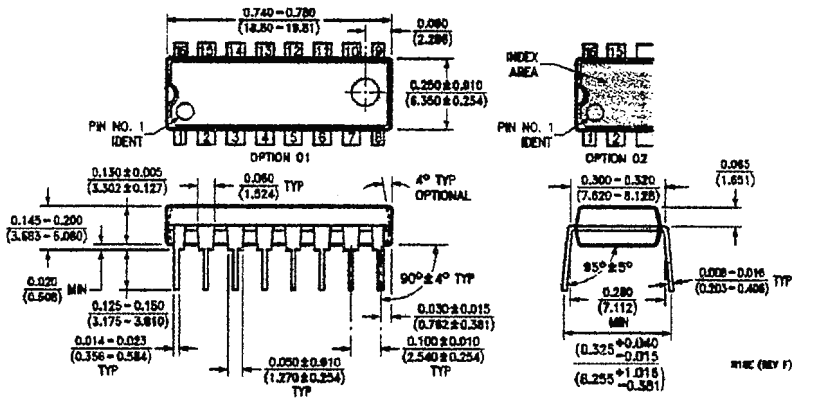
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD40192BMJ, CD40192BCJ, CD40193BMJ or CD40193BCJ
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number CD40192BMN, CD40192BCN, CD40193BMN or CD40193BCN
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

May 1995

54F/74F374
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

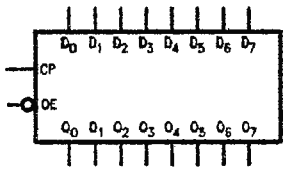
Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F374PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F374DM (QB)	J20A	20-Lead Ceramic Dual-In-Line
74F374SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F374SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
74F374MSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54F374FM (QB)	W20A	20-Lead Cerpack
	54F374LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

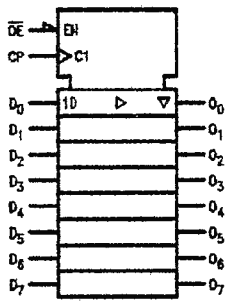
Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, and MSAX.

Logic Symbols



TL/F/9524–1

IEEE/IEC



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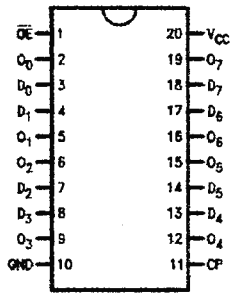
Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



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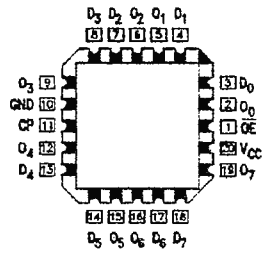
Pin Assignment for LCC



TL/F/9524–3

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RRD-B30M75/Printed in U. S. A.

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/−0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
O_0–O_7	TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)

Functional Description

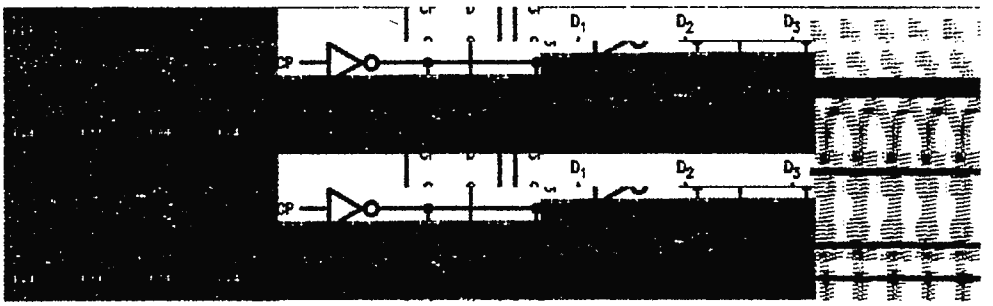
The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affected the state of the flip-flops.

Truth Table

Inputs			Internal Register	Output
D_n	CP	$\overline{OE}$		O_n
H	⌐	L	H	H
L	⌐	L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9524–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	140		60		70		MHz
t_{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns
t_{PHL}	CP to O_n	4.0	6.5	8.5	4.0	11.0	4.0	10.0	
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns
t_{PZL}		2.0	5.8	7.5	2.0	10.0	2.0	8.5	
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	ns
t_{PLZ}		1.5	4.3	5.5	1.5	7.5	1.5	6.5	

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	2.0		2.5		2.0		ns
$t_s(L)$	D_n to CP	2.0		2.0		2.0		
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_h(L)$	D_n to CP	2.0		2.5		2.0		
$t_w(H)$	CP Pulse Width	7.0		7.0		7.0		ns
$t_w(L)$	HIGH or LOW	6.0		6.0		6.0		

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 374 S C X

Temperature Range Family
- 74F = Commercial
- 54F = Military

Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier (LCC)
- S = Small Outline SOIC JEDEC
- SJ = Small Outline SOIC EIAJ
- MSA = Shrink Small Outline (EIAJ SSOP)

Temperature Range
- C = Commercial (0°C to +70°C)
- M = Military (−55°C to +125°C)

NOTE:
Not required for MSA package code

Special Variations
- QB = Military grade device with environmental and burn-in processing
- X = Devices shipped in 13" reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCZ}	Power Supply Current			55	86	mA	Max	V_O = HIGH Z